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Space Qualified Large Memory Array Implementation for a Solid State Recorder

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Abstract

This paper chronicles the design of a Solid State Recorder (SSR). The SSR's design was developed for the Goddard supported Command and Data Handling In Your Palm (C&DHIYP) project. The design was later modified and used for the Thermosphere * Ionosphere * Mesosphere * Energetics and Dynamics (TIMED) program. Commercial parts, principally DRAM and FPGAs which are susceptible to single event upset (SEU) from protons or heavy ion particles, dramatically influenced the SSR's design. Techniques for detecting and correcting SEUs in sensitive parts were extensively used; these included block error codes for data and voting hardware for logic.

I. INTRODUCTION

The SSR design started with the Goddard supported C&DHIYP In Your Palm project. This project is a packaging technology demonstration vehicle for bare die on a printer circuit board. [1] The system consists of two boards, a processor and a SSR. These boards form the core of the C&DHIYP system. Custom input/output boards are added to this core for program specific needs. Four months into the SSR design the TIMED mission began putting together their preliminary specifications. While not identical to C&DHIYP requirements they were close so adapting the C&DHIYP design to TIMED was a good choice.

In the following pages the effect of the two programs' specifications on the SSR design are discussed. In particular the impact of part selection and the requirement to have low or no data loss is described. Where appropriate the speed improvement that an ASIC implementation could achieve is discussed. The obvious boost in speed and decreased board real-estate make an ASIC controller implementation an attractive follow on to the present design.

II. SPECIFICATIONS

The SSR specifications for the C&DHIYP and TIMED board influenced the design approach. Both designs require that parts sensitive to SEU's should not impact data retention. Radiation test results for the Actel 1280's [2][3] show that only C-modules or triple voted S-modules are sufficiently insensitive to SEUs for most space missions. The no data loss requirement, coupled with the use of commercial DRAMs, to achieve sufficient capacity, means memory error correction is also needed.

The starting specifications from the C&DHIYP project are shown below. Because this program's main thrust was packaging, radiation concerns were secondary to using devices in bare die form.

A. *C&DHIYP Specifications*

- ≥1-gigabit capacity
- Random access for read and write
- Use stacked memory parts (Irvine Sensors [4] or TRW CI/Staktek [5] or Cubic [6])
- Actels FPGAs 1280, 1280A or 1280XL
- PCI or 1394 bus interface
- 4”x4” double sided boards
- No part latch up, No data loss, 10krads total dose
- 1Mbits/sec read/write

The TIMED mission requirements are:

B. *TIMED Specifications*

- ≥ 2-gigabit capacity
- Random access for read and write
- Actels FPGAs 1280A, commercial extended temperature range
- PCI bus
- Two 6”x8” single sided boards laminated back to back to a heat sink
- No part latch up, No data loss through South Atlantic Anomaly, 5krads total dose
- 100Kbits/sec write 4.5Mbits/sec read
- No bare die parts, conventional board assembly.

III. ACTEL INFLUENCE

Using commercial Actels FPGAs screened to program specific limits has been cost effective compared to more expensive radiation hard Actels. This is the direction that both C&DHIYP and TIMED took. This approach accepts the disadvantage that significant amount of design time will occur before the upscreening and radiation testing can take place.

A. Actel Radiation

Because of the requirement to recover 100% of the data and the unknown radiation specifications for both programs, all storage elements are triple voted and self refreshing (both C and S module flip flops). This is true for the core SSR controllers.

The SSR core controllers make use of Actel flip flops with enables in a synchronous design methodology. The Actel 1280 library includes S-modules flip flops with enables but lacks C-modules with simular structure. At the time of the design, available test data placed the S-module upset rate at $1.39 * 10^{-5}$ errors per device-sec and the C-module upset rate at $1.53 * 10^{-8}$ errors per device-sec [7]. In order to use the SEU susceptible S-modules, a self refreshing triple voted S-module flip flop was employed. The following error rate equation predicts the error rate for this type of flip flop. The equation was derived by Jim Kinnison [8] through the use of a Monte Carlo simulations and is valid for frequencies above 100kHz and with in the range of the 1280's clocking speed.

$$\text{(1)} \quad \text{Error Rate} = 6.46 * 10^{-6} * (F_c)^{-0.879}$$

Where the Error Rate is in Errors/Second, and the F_c is the update frequency in Hertz. Figure 1 is a plot of this equation adjusted for a year of operation. Note that for an operating frequency of 1MHz or better the expected number of errors is 0.001 per year per flip flop.

The SSR controllers use clock frequencies of 12Mhz, 6Mhz and 4Mhz. Taking into account each of the S-module flip flops and its clocking frequency, an SSR's yearly error rate of $6.7 * 10^{-2}$ is predicted for the core control FPGAs.

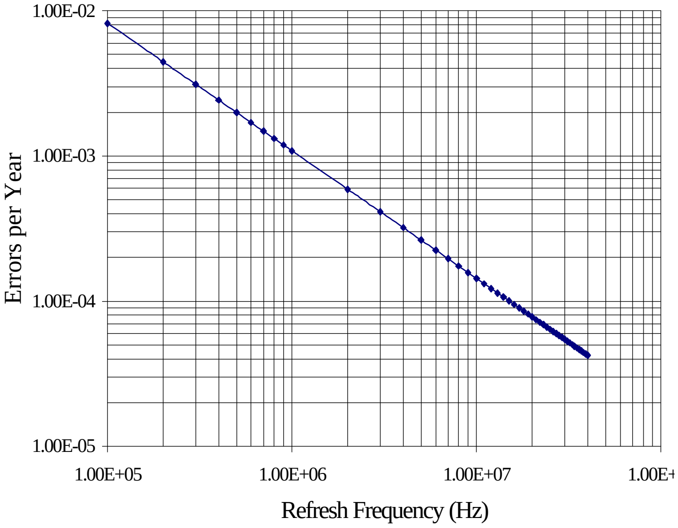

Figure 1: Triple vote S module error per year verses frequency of operation.

B. Actel Speed

Triple voted modules effected system clocking speed. The military worst case time of propagation through a triple voted flip flop made of C modules is 30 nsec. This does not take into account routing delay variation. Based on this number, the half cycle maximum clock rate was chosen to be 40 nsec. This frequency allows for use of both rising and falling edges of the clock. For both C&DHIYP and TIMED projects the available clock frequency closest to this limit was 12MHz. This number effects the memory access timing and is a good place where an ASIC can improve throughput.

The main triple voting circuits used in this design are shown in Figure 2 and 3. Figure 2 is a self refreshing S-module flip flop. Note that the voted data output is fed back to the input whenever the enable line is not active. There are only two module delays in this design and it uses only four modules total. This part is slightly slower than a single C-module flip flop.

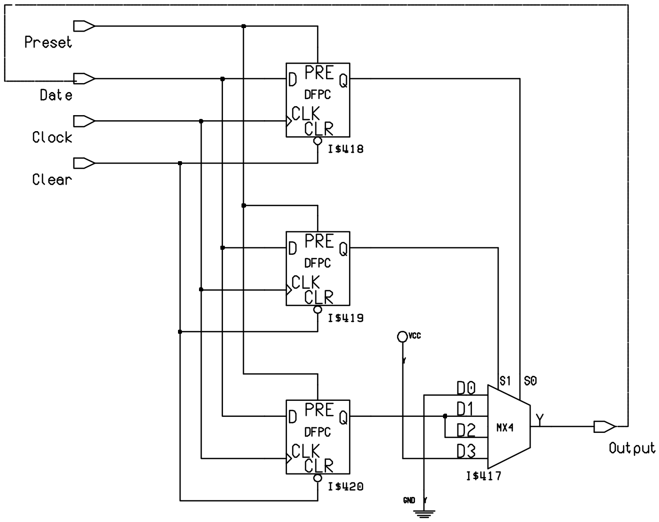

Figure 2: Triple voting self refreshing enable S module flip flop.

Figure 3 is the triple voted C-module flip flop. This flip flop is used as a self refresh set-reset logic element. It is an ideal long term storage element, with a probability of upset less then 10^{-14} errors per year.

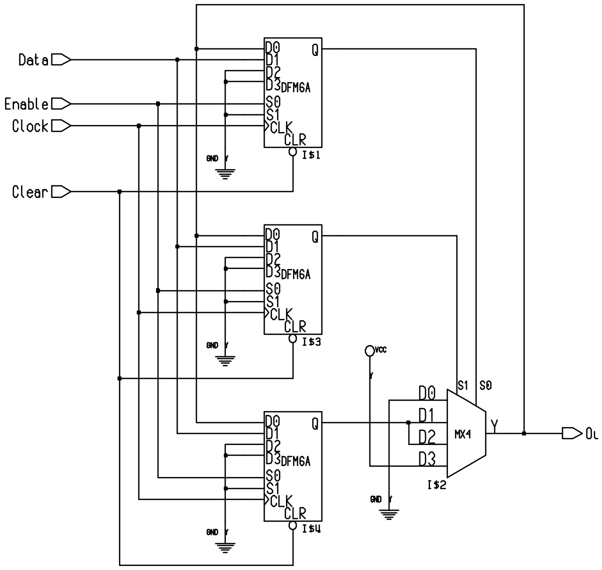

Figure 3: Triple voting C module connected as a self refreshing set-reset flip flop.

C. Actel Module Utilization

The Actel 1280 FPGAs contain 624 S-modules and 608 C-modules. Prior experience with triple voted designs have shown that 85% utilization will place well, even when pin outs have been specified prior to routing. Thus, for both C&DHIYP and TIMED the board layouts proceeded in parallel with detailed controller designs. Concurrent engineering was possible because interfaces were well defined early in the program. This approach allowed not only breadboards to be designed ahead of control logic but engineering board designs proceed ahead of breadboard testing. From breadboard to engineering board there only were two board changes. There was one additional track change between engineering and flight boards.

Table 1 gives the final utilization figures for the FPGA controllers in the TIMED SSR design. The PCI and the FIFO controller are replaced with the 1394 bus interface in the C&DHIYP design.

Table 1: Actel Controller Utilization

Controller	% Utilization
Read Block	73
Write Block	73
Byte	82
Memory Scrub	69
Dual Stack	98
Traffic Cop	35
FIFO Arbitration	30
PCI	69

IV. MEMORY INFLUENCE

The memory organization, refresh style (4k, 8k internal or external), packaging and radiation susceptibility of commercial DRAMs influenced the SSR design.

For the C&DHIYP program three different stacked DRAM modules were under consideration. Modules from Irvine Sensors made up of IBM Luna parts were the first that controller designs accommodated. Radiation tests of these parts indicated a very hard design. Unfortunately availability and cost placed these parts out of reach for both the C&DHIYP and TIMED programs. Another stacked DRAM module made by TRW used Samsung parts that had good SEU tolerance. The C&DHIYP project used 12 of these modules to get a total capacity of 1.6 Gbits.

The TIMED program chose denser Samsung 64Megbit, 3.3volt DRAMs. These parts allowed for conventional packaging techniques to meet the capacity requirement with a single board design. TIMED used 40 of the DRAM parts (~2.6Gigabits).

A. Memory SEU Rate

The TRW modules used in the C&DHIYP project are made up of eight 4Meg by 4bit Samsung DRAMs. The SEU error rate for the TRW stacks were not available until the exact part lot was determined. Test on previous lots indicated that the error rate should fall between 10^{-5} to 10^{-15} errors per bit-sec[9].

TIMED chose the Samsung[10] 64 Mbit DRAM. Based on the TIMED orbit, SEU testing [11] on the 64 Mbit parts showed a worst case proton upset rate of $3.4*10^{-10}$ errors per bit-sec. The error rate is high enough that an error correcting code more powerful then a simple double bit correction is needed to avoid excessive error scrubbing [12].

A survey turned up the University of New Mexico's [13][14] EDAC-5 chip. This is a byte oriented Reed Solomon encoder/decoder, that will correct five bytes in error, within a block that is up to 255 bytes long. The chip is manufactured in a radiation tolerant process and is used to improve the memory's expected error rate and hence reduce the scrub rate.

The 64 Megbit Samsung memories did not latchup for LETs as high as 48MeV/(mg/cm^2). Latchup would have complicated a no data loss design and will not be covered in this paper.

B. Memory Refresh Style

The memory refresh structures covered by the SSR's design are of the 4k and 8k type, where 4k/8k refers to a memory organization with 2^{12} or 2^{13} row addresses. The effect of accommodating both refresh rates is to require the memory address control logic to have programmable rollover points at 12 and 13 bits. This requirement effects the counters that keep track of the addresses and how long it takes to perform a refresh cycle.

The memory that C&DHIYP picked requires a refresh cycle every 128mSec while the memories chosen for TIMED have a maximum of 64 msec between refresh cycles. In order to guarantee a refresh cycle every 64 msec, a refresh cycle is requested every 32 msec by the control logic. Because no SEU data on the memory's internal refresh controller was available, RAS only external refresh was implemented. The clocking frequencies available to the SSR limited the external refresh clocking to 6MHz, or 1.365 msec per chip. In TIMEDs case this means 10 chips, refreshed two at a time with a total refresh time of 6.825 msec. The memory chips allow up to 10MHz external refresh clocking, µ820 Sec per chip or 4.1mSec for the group of 10 chips.

To ensure that memory refresh cycle requirements are met, the SSR design allows selecting the request clock's frequency and the number of clocks between request. The clock rates available are 4, 8, 16 or 32 msec per cycle. At a given clock rate, up to 31 counts are permitted. There is also the option to refresh one or two chips within a stack during each cycle. This feature allows peak power during refresh to be traded for speed of refresh.

The minimum time to refresh a stack can be improved through the use of clock frequencies that are closer to the maximum refresh rate. For the SSR design this will require faster FPGAs.

C. Memory Organization

The organization of the DRAM memories required the support of up to 8Meg by 8bits in groups of up to 10 chips. In fact the counters in the final design can support 64Meg by 8bits and up to 16 chips in a stack. These numbers are some what academic and must be checked against the maximum refresh rate of the memory and the ability of the controllers to support that rate.

V. EDAC-5 INFLUENCE

The EDAC-5 Reed Solomon encoder decoder is designed by the University of New Mexico's Microelectronics Research Center. This part allows the SSR to divide the memory into blocks 254-bytes long, where each block can tolerate up to 5-bytes in error. A byte error can have up to 8-bits in error. That is a block can have as many as 40-bits changed due to an SEU event and still recover all data, as long as no more then 5 bytes are effected.

A. EDAC-5 Operation

The SSR design has chosen to define each block as 254 bytes, 244 bytes of data and 10 error correcting bytes. To keep blocks on even memory partitions 2 bytes are not used. This produces a 95% memory data utilization factor. Three EDAC-5 chips are used in the SSR System; one each for read, write and scrub.

B. EDAC-5 Radiation Properties

The EDAC-5 chip is manufactured in a radiation tolerant process (> 20K rads total dose) and internally uses a single error correcting Hamming code. With an SEU threshold of LET=30MeV-cm^2/mg and a SEL threshold that excees LET=120MeV-cm^2/mg this part improves the memory's expected error rate depending on the scrub rate. For the TIMED mission, the scrub rate verses the probability of an unrecoverable block error is plotted in Figure 4. A memory error rate of $3.4*10^{-10}$ errors per bit-sec was used in the calculation.

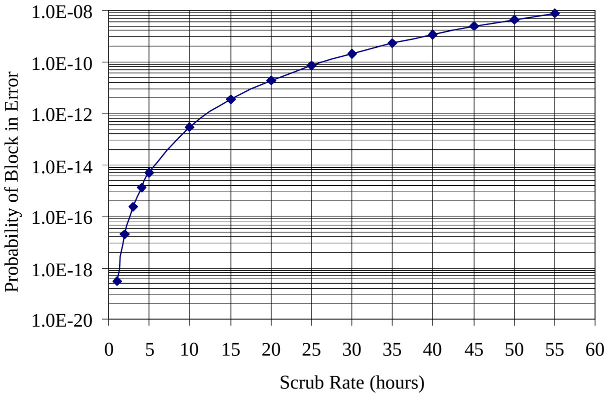

Figure 4: Block in Error Probability for a given Memory Scrub Rate.

C. *EDAC-5 Speed*

The EDAC-5 design is most efficient when streaming data through in either encoding or decoding mode. Once up and running the chip will process data at a 10Mbyte per second rate. Because of the random memory access requirement, the SSR is setup to pass one block at a time through the EDAC-5.

In the block mode it takes 845 clock cycles to move 244 data bytes into memory. Our system runs with a data clock of 4MHz. This sets the data rate through the EDAC-5 to 9.24 Mbits per second. With the refresh overhead (6.8mSec out of 32mSec) the throughput drops to 7.3Mbits per second. The actual measured rate, read or write, was 5.5Mbits per second because of the tasks arbitrating for the SSR resources.

If the controller logic permitted the maximum EDAC-5 clocking rate of 10MHz then the data rate through the EDAC-5 would become 23.1 Mbits per second. Subtracting off for the refresh overhead drops the data rate to 18.2 Mbits per second. With a 40% task arbitrating tax, the read/write data rate is still 10 Mbits per second. This is a good place where a ASIC or faster FPGA can improve performance.

VI. THE SYSTEM

The preceding discussion dwelled upon the primary influences on the SSR design. This section gives a brief description of the controllers developed for the SSR.

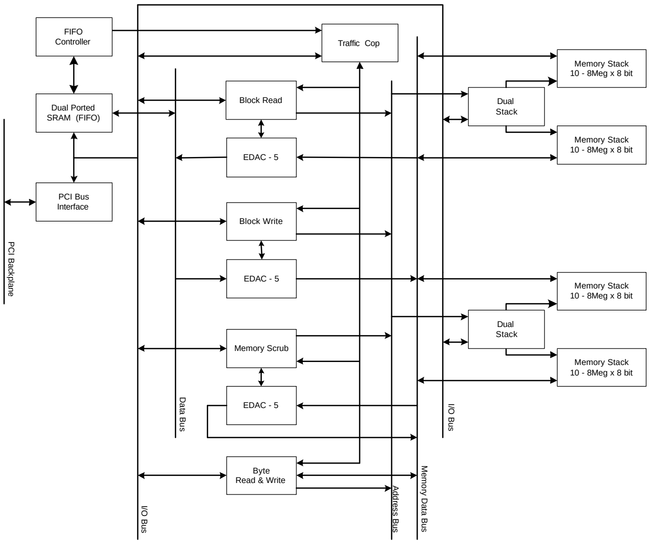

Figure 5: TIMED SSR Block Diagram

The design of a radiation tolerant memory array encompasses many considerations. Among those considerations are the size of the array, how the array is accessed and at what speed, parts available and how much real-estate is allotted for the design. For the SSR, the available parts were Actel FPGAs for controllers and commercial DRAMs. Figure 5 is the block diagram of the TIMED SSR. This design is based around a core set of controllers, each a single Actel 1280, to which a system bus controller is added. The C&DHIYP design is similar but replaces the PCI interface with a 1394 bus controller. For the C&DHIYP design the memory stacks are replaced with 12, TRW 8-high, 4 Meg by 4-bit modules, and a third dual stack controller is required.

The SSR controllers are partitioned by function into 6 Actel 1280s. The PCI system bus adds 2 more Actels. In general, the state machines of each controller are designed with no missing states. In this way, should an SEU event occur the most that will happen is the loss of one block of data.

A. *System Bus Controllers (PCI /1394)*

The SSR design allows for different system bus interfaces. This is accomplished through the use of a common interface definition with the user side of the system bus and the core SSR controllers. The interface uses a 5 bit address, 16 bit wide I/O bus and a 8 bit wide data bus. Data handshaking is handled with read and write strobes answered with an acknowledge strobe, indicating data transfer.

For the PCI design, the SSR I/O and data buses are implemented with independent handshake lines. In the 1394 implementation these buses are combined and a common set of handshakes are utilized.

B. Traffic Cop

The Traffic cop controller FPGA sets access priority to the internal SSR bus and memory. The pecking order is: Read, Write, Byte and then Scrub. This order is also a function of the requested memory stack's busy status. If the requested stack is in a refresh cycle, a controller requesting a different stack can take precedence over one higher in the pecking order. To ensure that no one function hogs memory, access is restricted to one block transfer for each request. Because the read and write controllers spend most of their time moving data to the output of the EDAC-5, there are large time gaps where another controller can take control of the memory.

C. Dual Stack Controller

The dual stack controller is responsible for refreshing two stacks of memory. This controller will issue a request to refresh at the selected rate. It is assumed this rate is one half of the memory's maximum refresh cycle time. If the memory is under control of the write, read, byte or scrub controllers the dual stack will wait up to one more scrub request cycle (32 millisec for TIMED and 64 millisec for C&DHIYP). During the second request cycle time the dual stack controller forces a refresh of the memory stack. The transfer in progress is interrupted and the controller will recycle. This ensures that data in memory is retained. The condition can only occur if either the refresh rate is set too fast or a controller has hung.

D. Read Block Controller

The read block controller will get a block of data from memory, pass the data through the EDAC-5, and place the data plus two bytes of status into the bus interface FIFO. The status bytes contains the number of errors and if they were correctable. The read memory block address is incremented and the next block is read from memory. In this manor, consecutive blocks of data are read from memory without additional setup time. However, this scheme implies that the EDAC-5 must be flushed and the read controller reset when accessing nonconsecutive blocks.

E. Write Block Controller

The write block controller moves data from the bus interface FIFO into the EDAC-5. Ten error checking bytes are added and the data is shifted to the output of the EDAC-5. A request for access to proper stack of memory is made. Once granted, the data is written into memory. The block address is incremented, and the controllers wait for the next block to process.

F. Byte Controller

The byte controller tests the read and write functions. This controller allows direct access to every byte of data in memory. By doing so intentional errors can be introduced.

G. Memory Scrub

The memory scrub controller indexes once through all of memory every time it is activated. Memory scrubbing has the lowest priority and may take a long time if other functions are active. On the TIMED SSR board, a complete memory scrub will take as little as 6 minutes. The memory scrub controller will hold the internal buses for the entire time it takes to read and write back a block of data. This prevents new data writes from corrupting data already in memory during the scrub.

VII. RESULTS

The major influence of using commercial parts to design a radiation tolerant large memory array is the SEU tolerance that array must achieve. The SSR design for the TIMED mission has been completed. The breadboard and engineering model boards are tested and are up and running. Flight boards are in fabrication and will undergo test in the near future. For the C&DHIYP project the SSR section is in breadboard test and flight boards are expected next year.

A. *SSR Core Specifications*

- 4Meg x 4, 8Meg x 8 and up to 32Meg x 8, 5 or 3.3 Volt DRAM storage elements allowed. Arranged in stacks of 8 or 10 chips. Up to 8 stacks. (supports a maximum of 80 memory chips).
- Block access to data is random to within 244 data bytes per block, for both read and write.
- Control logic is implemented with Actel 1280, 1280A or 1280XL FPGAs.
- PCI and the IEEE 1394 bus interfaces are supported.
- No radiation induced latch up. For TIMED, core controller yearly error rate of $6.7*10^{-2}$, probability of

block in error < 10^{-10} (no scrub 24 hour data retention). Total dose >15K Rads (Si).

- 5.5Mbits/sec read, 5.5Mbits/sec write with targeted controller parts.

VIII. ACKNOWLEDGMENTS

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IX. ACRONYMS

ASIC	Application Specific Integrated Circuit
C&DHIYP	Command and Data Handling In Your Palm
DRAM	Dynamic Random Access Memory
FIFO	First In First Out
FPGA	Field Programmable Gate Array
LET	Linear Energy Transfer
PCI	Peripheral Component Interconnect
RAS	Row Address Strobe
SEL	Single Event Latch
SEU	Single Event Upset
SSR	Solid State Recorder
TIMED	Thermosphere Ionosphere Mesosphere Energetics and Dynamics

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