Radiation Effects in the Aeroflex RadHard Anti-fuse FPGA

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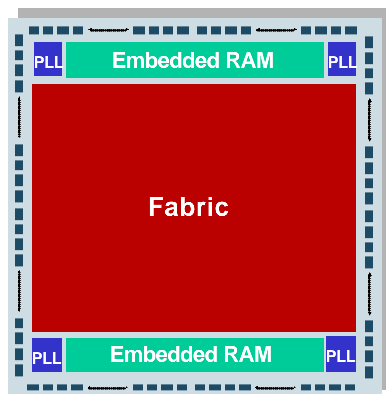
Abstract

Radiation testing on the Aeroflex's UTMC UT6325 RadHard FPGA is the focus of this paper. Testing on the QuickLogic QL6325 will be referenced to establish a baseline. Results from radiation testing on the Aeroflex UT6325 will then be discussed. UT6325 radiation testing will be broken into three specific discussions: total ionizing dose and its effect on delay structures, static SEL and dynamic SEU. SEL/SEU test structures will include the internal logic cell registers, the on-chip SRAM and the I/O registers.

Introduction

The space applications design community has presented many papers discussing the application of radiation-hardened-by-design techniques to commercial CMOS foundries [1-3]. Aeroflex has applied these established ideas, with proprietary enhancements, to the 0.25µm, CMOS shallow trench isolation process available at TSMC. Previous Aeroflex products have provided an opportunity to establish design and layout procedures for basic RAM and register structures [4-6]. Applying these proven structures to a redesign of the QuickLogic QL6325 anti-fuse FPGA created the Aeroflex UT6325. The underlying technology of the UT6325 RadHard FPGA can best be understood from referencing the QuickLogic Data Sheet and application notes available at their web-site [7]. For quick reference, the UT6325 (Figure 1) contains 1536 internal logic cells, 320 I/O buffers and 24 SRAM blocks.

Figure 1.
UT6325 Architecture



Each of the 1536 internal logic cells (Figure 2) contains a cloud of combinatorial logic and two RadHard flip-flops. The I/O buffers (Figure 3) are programmable to a variety of interfaces, and each I/O contains three additional RadHard flip-flops. The 24 RadHard SRAM blocks are configurable into four separate modes and may be cascaded for a total of 55,300 bits.

Figure 2.
Internal Logic Cell

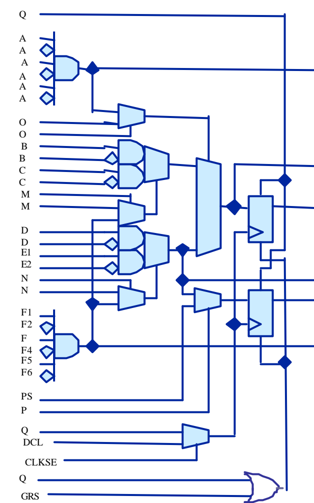
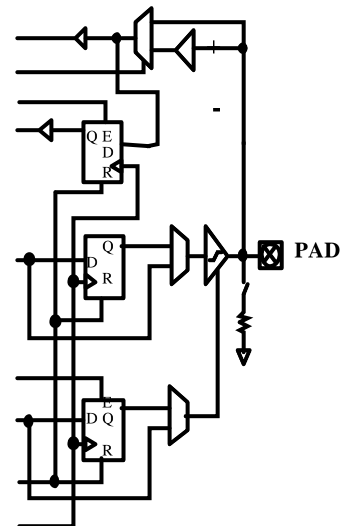


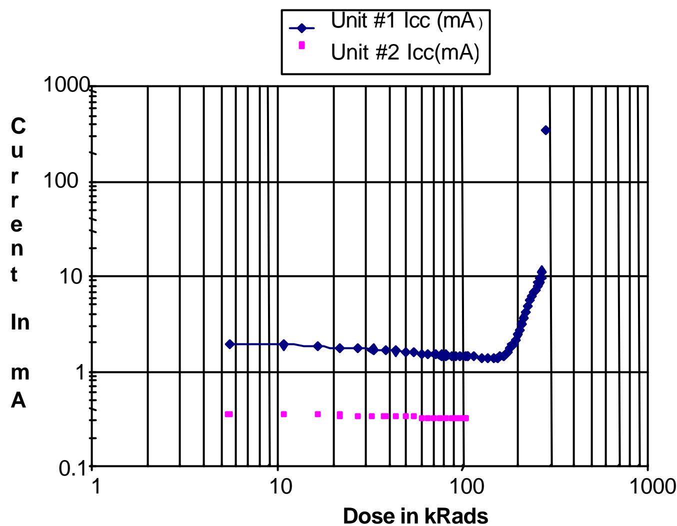
Figure 3.
I/O Buffer w/ Registers



Total Dose testing on the commercial QL6325 established this device exceeds the 100 krad TID goal with considerable margin (Figure 4). SEL testing on the QL6325 showed the onset of latch-up at a LET of 15 and a fluence of 1E5 ions. Thus, the redesign effort for the UT6325 focused on improving SEL and SEU performance. A brief discussion of the radiation-hardened-by-design effort will be followed by details on the specific test chips and test procedures in place for the UT6325. It is the intent of the author to describe the status of test preparation for a device currently undergoing final design review. The results of testing-to-date will be the focus of the presentation at the conference in September.

Figure 4.

Total Dose Krads versus Qidd QL6325

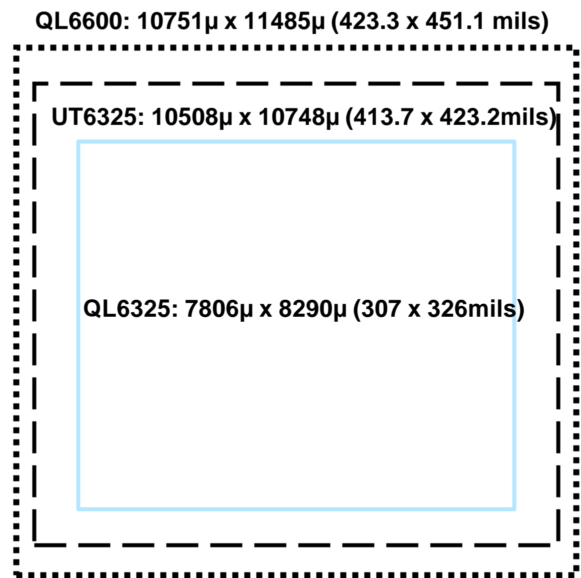


RadHard by Design FPGA Development

Aeroflex used design techniques commonly available within the industry, as well as company proprietary modifications to produce the UT6325. No modifications were made to the anti-fuse structure. This has been shown by QuickLogic to provide a reliable, fast method for the interconnection of FPGA wiring. However, considerable rework has been done to the design and layout of the transistor active areas, the creation of dually redundant flip flops, the layout of critical flip flop storage nodes and the power/ground busing.

Latch-up structures in the 0.25µm TSMC bulk CMOS on epitaxial silicon process are similar to those identified by others in the industry with other 0.25µm CMOS processes. Namely the latch-up state is caused by lateral and vertical parasitic transistors inherent in the CMOS manufacturing process. The gain of these parasitic bipolar transistors combined with their base-emitter resistance allows for a positive feedback, latch-up state to occur when internal transients are caused by high energy, heavy ion strikes. A variety of proprietary guard banding techniques for well / substrate ties have been developed. These are combined with enhancements to the physical layout and separation of the transistor devices to modify the base resistively and transistor gain. Again, while the general techniques are well understood in the industry, the exact size and spacing of the guard-bands, contacts, and implants are proprietary to Aeroflex. It can be stated the implementation of the LET mitigation techniques, as well as the insertion of dually redundant flip-flops for all register functions has caused the size of the UT6325 die to grow by approximately 20% over the sizing of its' commercial equivalent (Figure 5). This increase in die size was anticipated at Aeroflex and is, in fact, the reason that the smaller QL6325 device was chosen from the QuickLogic Eclipse family for modification. The growth of this die is below the size of the largest members of the family. Thus, programming currents for anti-fuses have been maintained within the established limits for this technology.

Figure 5.
UT6325 vs QL Die Sizes



To address the requirements for SEU tolerance, a new redundant latch structure was designed and used to replace all logic, memory, I/O and control circuitry latches. This latch design is similar to registers implemented in current Aeroflex ASIC and standard products. The latch uses a transistor redundancy scheme to duplicate storage of critical data on multiple register nodes. Rather than store registered data on two nodes as in commercial design, the master and slave portions of the latch store data on four nodes. Thus, an upset on any single node in the register is corrected by the data remaining on the other three nodes. The drive strength of the latch transistors for critical nodes has been increased to improve critical energy necessary to cause an upset. The physical layout of the latch cell has also been modified to separate redundant nodes to reduce the likelihood that a high-energy ion could effect more than a single node. The combination of these techniques allows the necessary threshold LET and upset rate for a RadHard FPGA.

Aeroflex is mitigating all SEL/SEU effects that impact the UT6325. This includes control circuitry present in the FPGA which, if upset, could cause device failures. The classic example is the power-on reset circuitry (POR). Aeroflex has experienced issues with this exact circuit in the design of other radiation-hardened product. Special care was taken to mitigate the POR by guard banding potential sites for SEL, inserting SEU immune dual registers and inserting circuitry to catch transient pulses. Other control functions that received full treatment for SEL/SEU effects include the mode control circuitry for unprogrammed FPGA test. These required attention to prevent the device from entering into a test mode after heavy ion strikes.

FPGA features that could not affect functional performance, such as the programming registers and JTAG, were mitigated for SEL only. These circuits were studied to verify they could be held in an inactive or reset mode during functional performance. While not affecting functionality, the registers must still be treated for SEL to mitigate for high currents effecting reliability and low power performance. The improvement for dose rate effects has been addressed through the redesign of the power and ground busses on the FPGA and the addition of extra contacts were appropriate in this bussing. Power and ground busses have been widened and routed on multiple layers to improve current density capabilities and device reliability.

Review of Design Goals

The goal of the RadHard FPGA development was to meet the radiation requirements for the majority of space level logic designs. See Table 1 for RadHard goals. The difference in threshold LET for logic and SRAM devices is explained by transient effects which exist only in the preset / clear circuitry for the logic flip flops. All flip flops contain the same redundant register design.

Table 1
Aeroflex UT6325 RadHard Test Goals

RadHard FPGA Goals	
Feature	**Performance**
-Total-dose	100Krad(Si)
-SEL Immunity	>100MeV –cm^2/mg
-SEU LET_{th} Logic	>20 MeV-cm2/mg
-SEU LET_{th} SRAM	>40 Mev-cm2/mg
-SEU error Rate	<1.0E-8 errors/bit-day

Testing time at Lawrence Berkeley Laboratory and Texas A&M University has been scheduled to verify SEL and SEU performance. Two designs for radiation effects testing have been completed using the QL6325 for debug. See Table 2 for design summary. Design R-1, emphasizing internal logic, SRAM modules and bi-directional I/O, has been created for total dose testing. Design R-1 was used to verify the TID tolerance of the QL6325 using a Cobalt-60 gamma source. This same design will be repeated on the UT6325 to verify the TID tolerance level and the effect of this dose on a variety of delay structures. See Table 3 for a list of TID delay structures. Design R-2, emphasizing register resources in logic cells, SRAM and I/O, is available for SEL / SEU analysis. This second design was used on the QL6325 to baseline its' latch-up tolerance to heavy ion bombardment. Testing radiation characteristics of the QuickLogic QL6325 allowed Aeroflex to complete the infrastructure necessary for the characterization of the RadHard UT6325. Designs, tester hardware and test program development are in place. All techniques have been verified to provide results on the commercial product. Final data for the UT6325 will be presented in the paper.

Table 2.
Designs for Radiation Tests

Design R-1	Design R-2
Testing	*Testing*
-TID	-SEL / SEU
- krad tolerance	-Register Control SET
- delay characterization	-Dedicated Clock SET

Table 3.
Radiation Effects Delay Chains

Element	Length
Inverter	750 250 w/ HDPAD 250 w/ CLKPAD
Multiplexor	500
NAND	250
Counter	dedicated clock programmable clock

Upcoming Test Requirements

The radiation characterization for the commercial device is complete. All infrastructure for these designs has been debugged using commercial parts. Programming adapters, tester programs, tester load boards, burn-in boards and

oven modifications have all been debugged with QL6325 parts. Comparable testing for the UT6325 has been scheduled. The results of this analysis will be presented in the final paper.

Summary

A commercial anti-fuse FPGA fabricated on the TSMC 0.25um, shallow trench isolation process has been radiation-hardened-by-design at Aeroflex. Using standard techniques, but with proprietary enhancements Aeroflex has focused redesign to address SEL/SEU effects. All register functions were included logic cells, SRAM and I/O registers all received similar treatment. Control circuitry for POR and test mode control was redesigned to mitigate radiation effects and prevent functional upset. Power/ground bussing was improved. Testing and characterization flows have been debugged using the original QL6325 commercial FPGA from QuickLogic. Test results for the RadHard UT6325 will be presented.

[1] Ronald C. Lacoe, Jon V. Osborn, Rocky Koga, Stephanie Brown, and Donald C. Mayer, "Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies", IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pp. 2334-2341.

[2] J. V. Osborn, D. C. Mayer, R. C. Lacoe, S. C. Moss, and S. D. LaLumondiere, "Single Event Latchup Characteristics of Three Commercial CMOS Processes," Pro. Of 7th NASA Symp. On VLSI Design, 1998, 4.3.1.

[3] J. V. Osborn, R. C. Lacoe, D. C. Mayer, and G. Yabiku, "Total Dose Hardness of Three Commercial CMOS Microelectronic Foundries," IEEE Trans. Nucl. Sci., vol. 45, 1998.

[4] J.M. Benedetto and D.B. Kerwin, "Total Dose Hardening of a Deep Sub-Micron Process for Mixed-Signal Applications", GOMAC Digest of Papers, 2001, pp. 539-542.

[5] J.M. Benedetto, "Single Event Effects and Prompt Dose Hardness of a Deep Sub-Micron Commercial Process", IEEE Radiation Effects Data Workshop, in Phoenix, Arizona, July 15, 2002, pp. 58-61.

[6] J.M. Benedetto, "Single Event Effects Analysis of an Advanced Synchronous Dynamic Random Access Memory (SDRAM)", RADECS 2002.

[7] www.quicklogic.com, QuickLogic Inc., home page for web site.