

Implementing a Rad-Hard Compact PCI bus-based system using Actel FPGAs

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The Electronic Systems Branch at the NASA Langley Research Center (LaRC) is developing the Control Module (CM) for the Geosynchronous Imaging Fourier Transform Spectrometer (GIFTS) satellite system. The CM consists of 5 major subsystems, the Instrument Controller (IC), the Memory board, the Downlink board, the I/O board, and the Engineering Data Subsystem (EDS) board. All of these boards are based on the compact PCI (cPCI) bus standard. Engineers at LaRC are implementing the EDS board, Memory board, and the I/O board in-house.

To implement the cPCI interface for each of the boards, the designers are using the cPCI cores available from Actel Corporation for implementation it in their RT54SX-S Field Programmable Gate Array (FPGA) device. The Actel PCI cores are synthesizable VHDL descriptions that implement the full Master and Target cPCI functionality, including DMA transfers. The EDS board is a simple PCI Target interface that allows the IC to read the health and status information over the PCI bus that it has gathered using its on-board AD converters. The I/O board is also a simple PCI Target that allows the IC to send and receive information from the sensors and spacecraft over the PCI bus before it is translated and forwarded over the proper external communications link. The Memory board is a full PCI Master + Target and uses the DMA capability to send image information from the sensor to the Downlink board for transmission to the ground.

The Memory board, I/O board, and EDS board designs use the Actel PCI core as a starting point and then add the additional functionality required for the individual board's function. In the case of the EDS board, the additional digital functions are minimal, and those and the PCI core can be fit into a single Actel FPGA. The functions of the memory board are complex enough that, in addition to 4Mbytes of rad-hard SRAM, it requires a total of three Actel FPGAs for implementation.

The designs for the Memory, I/O, and EDS boards are being developed using the Actel Libero Integrated Development Environment (IDE). The Libero IDE includes VHDL authoring tools and file management functionality, the ModelSim tool from Model Technology for VHDL functional and timing simulation, and the Synplify tool from Synplicity for gate-level synthesis from behavioral VHDL.

This paper will present the results of designing the cPCI-based boards for the GIFTS CM using VHDL synthesis and Actel FPGAs. The overall architecture of the most complex board, the

Memory board will be presented. The VHDL-based design methodology will be described as well as the functional and post-layout timing simulation methods employed. Major problems with the implementation technology, tools, and IP cores will be described as well as methods that were used to overcome them. Results of testing of initial physical prototypes of cPCI-based boards using Actel FPGAs will be discussed.