

Jitter, Power Integrity, and Proper PDS Design For FPGA Systems

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This paper will address the topic of jitter, its relationship with power integrity, and the techniques and concerns involved with the creation of an adequate Power Distribution System. A discussion on jitter, its sources, and its adverse affects on system timing and operation will set the table. This will lead into an exploration of decoupling capacitance and inductance of the distribution system under the topic of power integrity. The use of analytical methods and simulation techniques in order to design for reduced power supply noise and jitter will complete the paper under the topic of proper PDS design.