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Title: Consequences and Categories of SRAM FPGA
Configuration SEUs

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Consequences and Categories of SRAM FPGA Configuration SEUs

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Abstract

Ongoing projects at Los Alamos National Laboratory are planning to use SRAM based FPGAs in satellite applications to realize the benefits of reconfigurable computing. This allows on the fly reconfiguration of the hardware and supercomputer performance for processing remote sensing data. SEUs are one challenge to using this technology in space. An SEU simulator has been built and extensively tested against data collected in a proton accelerator. The simulator can quickly test a logic design and find bits in the FPGA configuration bitstream that cause functional failures. This paper discusses the functional categories of these critical bits for two designs. The probability of failure for these bits will also be shown. With this data, efforts to improve reliability can be directed against those bits in the configuration which most frequently cause errors.

The figure below is a zoomed diagram of the configuration bitstream showing critical bits color coded by the probability that when upset, they will cause a functional failure. Obviously these results are heavily dependent on the duration the upset is allowed to persist as well as the quality of the input test vectors. What is clear, however, is that the majority of bits that ever (as far as we can detect) cause functional failures ALWAYS cause failures. Figure 2 illustrates that for this multiplier test design, more than 60% of bits that cause errors do so 100% of the time that they are upset. This suggests that the performance of a system incorporating these devices may be significantly improved by mitigating the consequences of these super critical configuration bits.

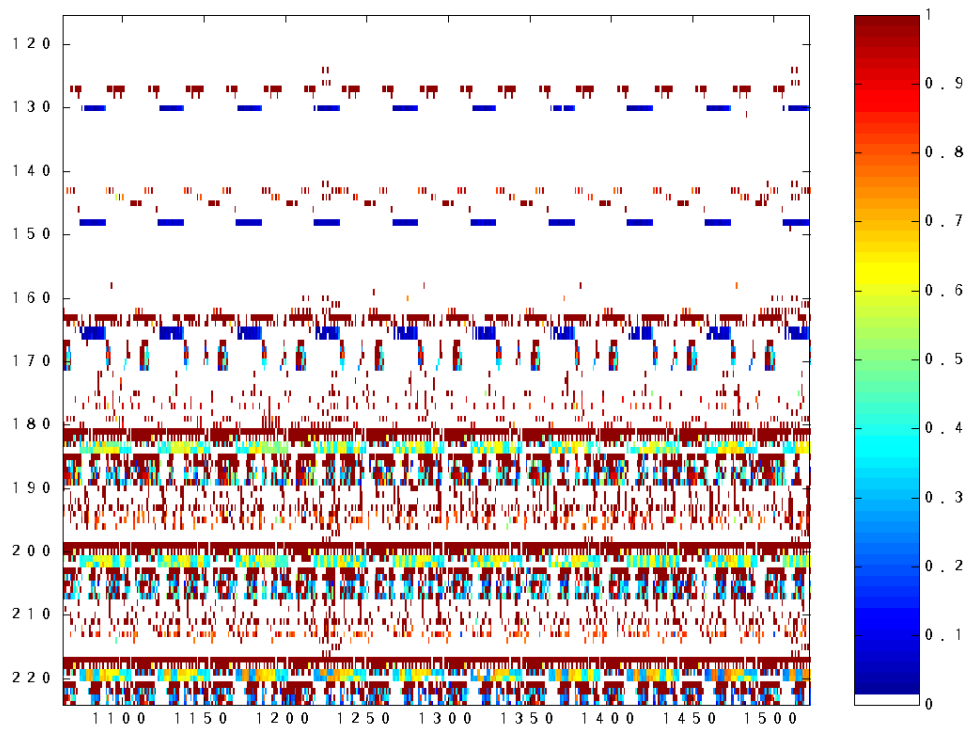
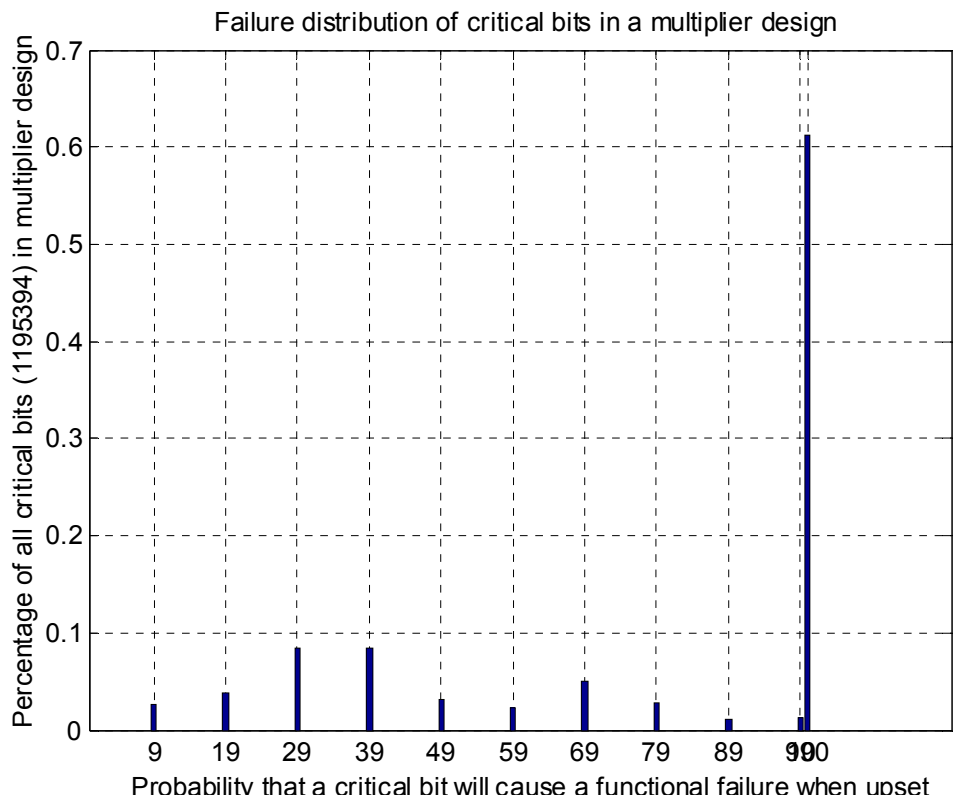


Figure 1: zoomed image of the virtex device multiplier test design bitstream showing the probability that a given bit will cause a functional error.



| Figure2: distribution of critical bits for the virtex multiplier design. Note that 60% of the configuration bits that ever cause errors generate them 100% of the time. This represents 78% of the 'design' sensitive cross-section.

A preliminary analysis of the critical bits for the multiplier design suggests that routing function dominates:

Routing: (79.7%)
Logic : (18.2%)
I/O : (1.9%)
Other : (0.2%)

The full paper will examine more designs and analyze those bits specifically which cause errors 100% of the time.

References

Caffrey, M., et al "A Space-Based Reconfigurable Radio," Military and Aerospace Applications of Programmable Logic Devices (MAPLD), 9/2002, Laurel MD.

Wirthlin, M. et al, "The Reliability of FPGA Circuit Designs in the Presence of Radiation Induced Configuration Upsets," IEEE symposium on Field-Programmable Custom Computing Machines 4/03, Napa CA.