EEPROM Bit Failure Investigation

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Introduction:

Two EEPROM single bit failures were reported by a recent JPL space mission. One failure was observed approximately six months into flight and the second bit failure approximately seven months later. The two bit failures were located in the same physical MCM package but different dies. In both cases, the contents changed from "0" to "1", i.e. from charged state to discharged state. This presentation summarizes the reliability investigation of these EEPROM single bit failures.

Reliability Analysis and Experimental Details:

A statistic reliability analysis on the EEPROM bit failures has been performed based on the EEPROM data sheet and its reliability report provided by the manufacturer. The analysis shows that an intrinsic EEPROM data retention bit failure should not be expected within the first six years of operation under operating condition of 50°C to 60°C, which was the temperature of the mission observing the two bit failures. However, an extrinsic bit failure resulting from a weak cell can happen any time before an intrinsic bit failure occurs. Furthermore, because of process induced and/or poorly programmed extrinsic reliability characteristics, weak cells may have several order of magnitude lower data retention or endurance lifetime and much higher failure rate and cannot be predicted in most cases. The basics of failure mechanisms for weak cells are the same as that for nominal cells, but the activation energy may be much lower and therefore weak cells are more susceptible to high temperature operation. We believe that the weak cells, either process induced or poorly programmed, may be the root cause of failures.

In order to investigate the reliability characteristics and obtain the activation energy of the weak cells, a diagnostic and write/read cycle testing plan was designed by modulating the write voltage externally to emulate weak cells. The experiment was performed on EEPROM chips from the same manufacturer. In the study, we have demonstrated that weak cells fail earlier and have lower activation energy as we expected. Nominal cells can become weak cells if the memory chip is not operated properly.

Conclusion:

We have concluded that “weak cells”, due to either process-induced defective cells or poorly programmed cells, may be the root cause of the bit and page failures observed, since the statistic reliability analysis on the EEPROM indicates that an intrinsic EEPROM data retention bit failure should not be expected within the first year of operation under 60°C. Diagnostic and write/read cycle testing to emulate weak cells were designed and performed to demonstrate that weak cells can fail earlier than a properly programmed array and that nominal cells can become weak cells if the memory chip is not programmed or operated properly. Read cycles can accelerate data retention failures on these weak cells. We have also concluded that the program timing of the EEPROM is very sensitive and that board timing margins need to be extensively analyzed to avoid possible program timing induced weak cells, which in turn may become early bit failures. It is necessary to point out that since the failed bits on the mission which observed the bit failure were not re-written, we can not verify our hypothesis with an actual failed part.