

## **FPGA Redesign of a Microprocessor-based Subsystem With no Impact to the Mission Software**

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### **Introduction: The Potential Impact of Microprocessor Obsolescence**

Rapid growth in microelectronics has been the enabling technology that allows military systems to perform functions never imagined. It is this same rapid growth, however, that has also created a large dilemma for the military. The life-time of a military system routinely extends 25 to 30 years and beyond, as opposed to a 4 to 7 year support cycle for commercial electronics. Additionally, microelectronic components become obsolete in as little as 12 to 18 months as they are replaced by faster, denser, and more complex technology. The impact is particularly extensive when a microprocessor hosting millions of dollars worth of development software becomes obsolete. Military systems take years to develop, at enormous costs, and are expected to last many years. The throw-away business model often used in the commercial world is unacceptable for these systems. Is there a reasonable solution?

In 2001, Raytheon Electronic Systems of Tucson Arizona was notified that two key ASIC devices within the Evolved Sea Sparrow Missile (ESSM), including a custom microprocessor, were no longer in production and no alternate sources were available. The Defense Microelectronics Activity applied a unique and innovative methodology to redesign the obsolete microprocessor with a 100% software compatible FPGA replacement. This briefing will present the specific methodology and techniques applied to successfully redesign the microprocessor using a Xilinx Virtex FPGA. The presentation will illustrate key steps, including characterization of the original microprocessor, implementation of the design, and verification that the redesign is 100% software compliant.

### **Development of the Microprocessor Specification: Vector Extraction**

Development of a comprehensive specification of the original microprocessor is critical to the redesign. The FPGA implementation must not only be functionally compatible, but also meet timing, including a match of clock cycles for the full instruction set. Additionally, self-test, power-up sequences, interrupts, etc. must all be taken into account.

Schematics and specifications from the vendor are a good starting point but often inaccurate or incomplete. DMEA used both the original schematic documentation and a physical legacy microprocessor to develop the redesign specification. The only sure method to precisely document the microprocessor is to exercise the physical part itself. This unique step was critical to ensure creation of an accurate specification.

DMEA developed a custom interface adapter which enabled mounting of the microprocessor to a chip tester. A series of test vectors were then driven into the device and the output vectors extracted. This was required for every instruction, including all addressing modes. Over 20 million test vectors formed the basis for a comprehensive characterization of the obsolete Raytheon microprocessor.

## **FPGA Redesign & Simulation**

DMEA selected the Xilinx Virtex XCV300 FPGA to replace the obsolete microprocessor. One obvious criteria in FPGA selection is meeting the environmental requirements of the missile. Another important feature of the component is 5V TTL I/O tolerance. The replacement FPGA will be required to function within the existing 5V missile system.

The key design functions were as follows:

- Design Entry: Various schematics of the Raytheon custom microprocessor existed, although accuracy and completeness was suspect. DMEA used these as a starting point for the redesign. The design entry evolved into both schematics and VHDL. Schematic entry was used where standard components within the Xilinx library matched the existing components. Many of the functions, however, were algorithms that did not have a component model available (e.g. 16 x 16 multiplier). VHDL code was developed to represent these functions.
- Simulation of Vectors created by Design Team: More than 80% of the design hours were spent on simulation. Model Technology and Synopsys simulators were used. The design engineers generated test benches as the design was entered. Test benches created in this phase mirrored the design engineer's interpretation of the schematic functions.
- Simulation of Vectors Extracted from Legacy Microprocessor: This is the heart and sole of the microprocessor redesign. Vectors extracted from the physical device during the characterization phase were converted and ported to the simulation tools. Test vector files totaling over 20M bits were applied to the simulators. The vector files provide both functional and timing information, with timing being the most difficult to match. The Virtex FPGA technology is considerably faster than the original custom Raytheon technology. A simple example is the insertion of buffer chains to create signal delay in the original design. To replicate this component-by-component in the Xilinx would not create the same delay and result in timing errors. The extracted vectors, however, provide precise timing data that enabled the design team to accurately match signal timing within the FPGA .

## **FPGA Hardware Test**

DMEA engineers designed a custom test adapter to interface a stand-alone XCV300 daughter board directly to the IMS tester. The test vector files extracted from the legacy microprocessor were applied to the XCV300 board. The output vectors of both microprocessor implementations were then ported to a spreadsheet for comparison. Discrepancies were flagged and sent to the design team for evaluation. The re-programmable attributes of FPGAs were invaluable for this aspect of the design. Design modifications were rapidly implemented and re-tested on the IMS tester. The final step was integrating the Xilinx FPGA into the original microprocessor module. DMEA designed a new layout of the module to accommodate the XCV300 as a replacement of the original microprocessor, but all other logic remained unchanged. The new CPU modules became form, fit, and functional direct replacements at the card level. Final system test was performed at Raytheon.

## **Summary**

Managers of long-life systems like those found in the military, NASA, commercial aircraft industry, etc. are faced with difficult challenges when microelectronic devices become obsolete. The problem is ten-fold when the obsolescence occurs to a microprocessor hosting software costing millions of dollars to development. DMEA has successfully developed a methodology utilizing programmable logic that can result in considerable time and cost savings. Implementing an FPGA version of an obsolete microprocessor can be a difficult task, but in many cases is the optimum solution.