A Configurable Architecture for High-Speed Communication Systems

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Abstract

Broadband wireless communications system design presents several unique challenges to the designer. The rapid emergence of new standards and technologies in this area has reduced not only the time to market but also the lifetime of products. A configurable architecture that is flexible enough to adapt to changes in specifications or standards is now necessary. This paper presents the experiences derived from the design of a prototype for an Emergency Response Gateway of a rapidly deployable "last mile" wireless high-speed communications system to support emergency management[1].

I. INTRODUCTION

Broadband wireless technologies have the potential to provide integrated data and multimedia services in several niche areas. There is a growing need to develop high performance communication systems that can satisfy high-end data processing requirements inherent in these technologies.

Designers of broadband wireless communication systems face the following challenges:

- Several difficult, and interesting issues related to access mechanisms, error rates, transmission rates and bandwidth need to be addressed
- High-level protocol descriptions have to be rapidly translated into hardware and software that realize the system
- A thorough test and verification process must be completed within shrinking time-to-market windows
- Risk of costly hardware and software redesigns must be minimized

Moreover the system design must be capable of adapting to late changes in specification or emerging standards. The speed and complexity of these systems necessitates designers to break away from traditional architectures and design methodologies. Designers must leverage new technology and resources like specialized Communication and Networking processors and High density FPGAs to achieve rapid system level prototyping. Field-programmable gate arrays (FPGA) offer an attractive alternative to the low efficiency of Digital Signal Processors (DSP) based systems and low flexibility of Application Specific Integrated Circuits (ASIC). The availability of high-density, high performance field-programmable gate arrays with several capabilities, like embedded memory and advanced routing, together with the adaptability that they offer make them highly desirable for developing hardware prototypes of communication systems.

II. EMERGENCY RESPONSE COMMUNICATIONS

In a typical disaster area most or all communications are usually wiped out. Field workers responding to emergency or disaster situations are often handicapped by the absence of communications infrastructure. A high data rate (up to 120 Mbps) system has been designed [1] incorporating innovative features that support rapid deployment and robust operation, including a built-in channel sounder and adaptive link layer protocols. The system utilizes surviving network infrastructure to provide network connectivity to field workers responding to emergencies or disasters for applications such as Internet Access, Audio/Video conferencing, Geographic Information System (GIS) access.

A. Network Topology

The network topology consists of a base station or hub and up to eight field units or remotes. The prototype network topology with a hub and two remotes is shown in Figure 1 below.

The base station or hub has a high data rate connection to the surviving terrestrial network. Where this is not possible a high data rate satellite-based connection can be used instead. The hub "illuminates" disaster area with 120 Mbps connectivity using broadband wireless. Geographic design tools assure that the coverage is as complete as possible. The field units provide personal digital assistants (PDAs) or laptops carried by field personnel with LAN services ranging from 10/100 Mbps Ethernet to IEEE 802.11 wireless connectivity.

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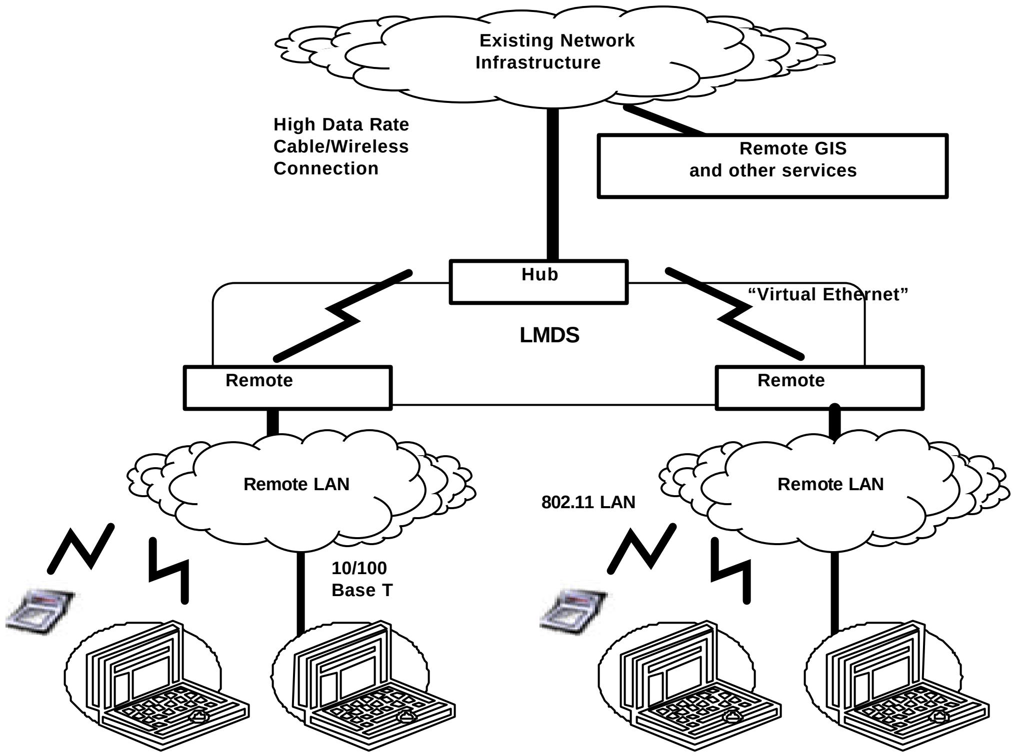

Figure 1 Emergency Response Communications Network Topology

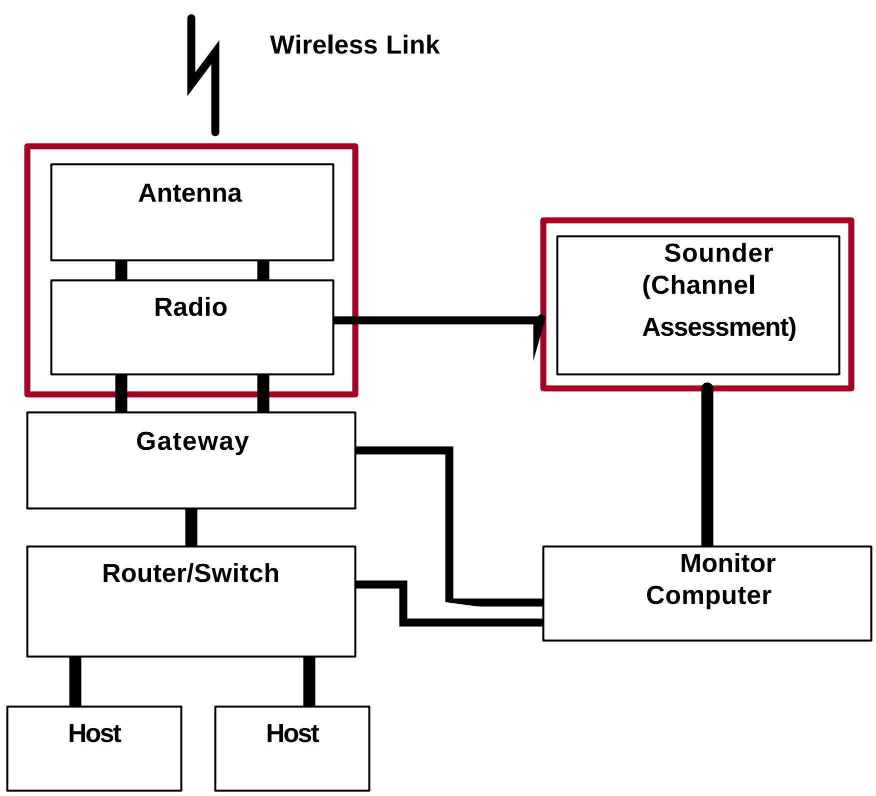

Figure 2 Emergency Response Communication System Overview

B. System Overview

The high data rate (up to 120 Mbps) system is designed to incorporate innovative features that support rapid deployment and robust operation, including a built-in channel sounder and adaptive link layer protocols. The broadband sounder unit helps in the initial 'site-ing' and performs continued channel assessment. GIS applications running in the monitor computer provides a view shed analysis and helps in rapid site planning. An overview of the system components with respect to the Gateway unit is shown in Fig.2.

III. CONFIGURABLE ARCHITECTURE FOR COMMUNICATION SYSTEMS

This section presents the configurable architecture applied to the development of the broadband wireless Gateway prototype.

A. Need for Configurable Architectures

The simplest and most common architecture used in traditional designs is to use a microprocessor or DSP with a set of application specific peripherals. In this scenario all the system blocks are mapped to software running on the processor or DSP. Though this provides a lot of flexibility the serial processing model of software-based design limits system performance to a great extent. Also DSPs may not be as attractive in cycle intensive operations like error correction algorithms and filters where hardware implementations tend to be more efficient.

On the other end of the spectrum, ASICs yield very high performance but require significant NRE cost and effort. ASICs offer no flexibility to the designer and require tremendous redesign efforts in the face of changing specifications or standard updates. This makes the ASIC option unsuitable for the development of applications that are based on standards that have not yet stabilized or undergoing development – a trend that is common in today's industry.

B. Configurable Architecture for Communication Systems

Most communication system designs implement a complex wireless multiple access MAC schemes and wire line network interfaces. Various physical layer adaptation techniques commonly implemented in wireless systems like variable forward error correction (FEC) and link-level automatic repeat request (ARQ) capability offer additional complexity at these high speeds. The emergency response gateway, for example, is capable of handling data rates up to 120 Mbps. Given, the high bandwidth, processing complexity and the volume of data that needs to be transported between constituent blocks, traditional bus based architectures are not viable. These designs have both packet level and bit level processing requirements. Packet level data processing is most efficiently performed using software where as bit level processing favors hardware implementations. Given these requirements a combination of specialized processor for packet level operations and programmable logic devices like FPGAs for bit level operations offer an excellent alternative. High density FPGAs and readily available configurable IP cores provide significant performance improvement by allowing designers to take advantage of parallelism and pipelining processing stages.

The architectural elements can be broadly classified as control or data path elements. The control elements deal with timing, status and ordering functions. These elements are implemented in the processor. The data path elements consist of functions that move, alter or add to the data that is transmitted or received. The data path elements can be further classified into:

- "Functional Units" (FU) which modify or transform data
- multiple scattered DMA-like "Processing Elements" (PE) that move data
- embedded and external "Memory Units" (MU) to store data between stages.

The functional units perform various stages of the data processing before transmission and after reception. Forward error correction codecs or modulation symbol mappers are examples of Functional Units. The processing elements perform data transfers between data processing stages or functional units. The architecture is designed to be memory centric in that distributed memory elements like buffers or FIFOs exist between each functional stage of the data path.

Figure 3 shows a generic memory centric configurable architecture design showing possible arrangements of the three generic data path elements. A dual port memory between the microprocessor and other processing elements allows simultaneous reads and writes. This modular architecture permits designers to take greater advantage of IP core reuse and further simplifies interfaces to promote easier integration of heterogeneous system blocks.

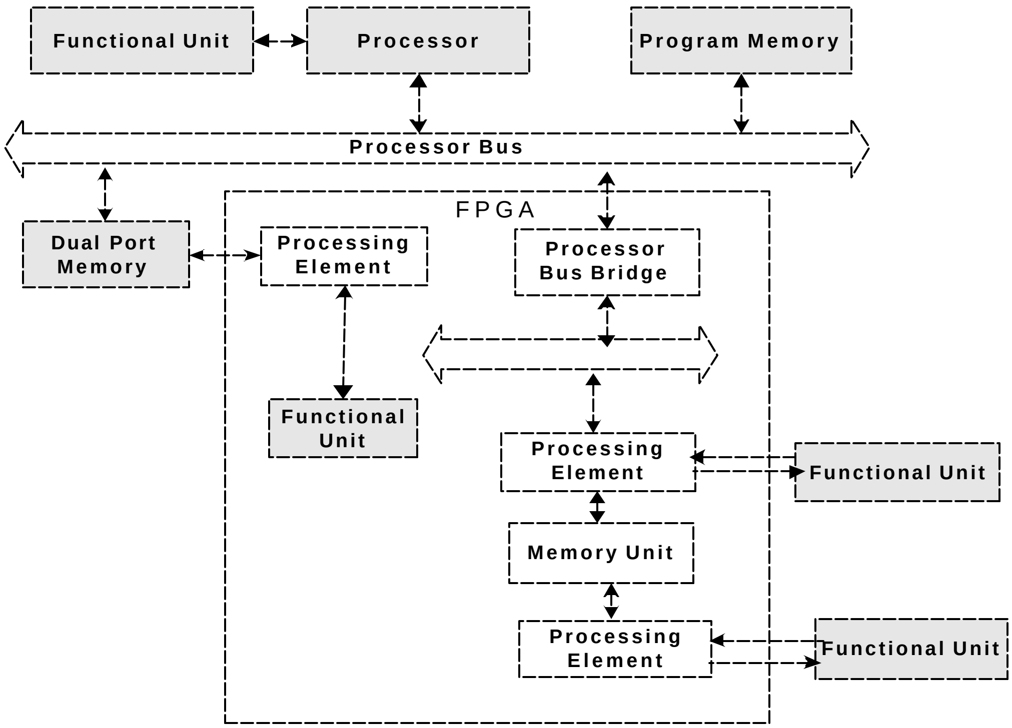

Figure 3 Generic memory-centric configurable architecture

IV. Disaster Response Communications Gateway Prototype Design

The Disaster Response Communications Gateway implements 100 Mbps Fast Ethernet and LMDS radio interfaces. It implements a time division multiple access MAC protocol in a star configuration allowing bi-directional data transfer. The Gateway design implements link level adaptation techniques like adaptive Forward Error Correction (FEC) and optional link level Automatic Repeat Request (ARQ) capability to trade off error rates and transmission rates. Simulations were performed using MATLAB [2] and OPNET Modeler [3] to determine the effect of FEC coding levels and to select suitable ARQ schemes. Four fixed coding levels were selected so as to provide a dynamic tradeoff between data rates and bit error rates.

The medium access protocol implemented involves packet processing, segmentation and reassembly. A FPGA centric architecture with multiple scattered Processing Elements (PE) structures and Memory Elements (ME) that take advantage of parallelism to cascade data between the processing stages or Functional Units (FU) is proposed, thus reducing processor load. The processing elements are implemented partly in software and partly in FPGA hardware. The mapping functional units was based on performance tradeoffs as well as cost considerations. For example the Turbo Product Encoder and Decoder were implemented in ASICs instead of IP cores mainly due to the cost and availability limitations associated with the particular IP cores.

A common approach during prototyping is to use a combination of a general-purpose processor (GPP) and a FPGA. However as the data rates increase general-purpose processors may not provide the desired performance forcing designers to implement logic in ASICs. The long design time and NRE associated with ASICs may not be suitable to implement new protocols that may be evolving or undergoing standardization. In contrast, Network/Communication processor platforms are optimized to perform "packet processing" operations [4]. The computational power required is determined not only by the data rate, but also by the packet processing operations that are to be performed. These specialized processor platforms also have built in protocol interfaces that simplify the design for the communication system designer. For example standard interfaces like Media Independent Interface (MII) for Ethernet or UTOPIA Interfaces for Asynchronous Transfer Mode (ATM) are supported by most of these processors. In designs that have energy restrictions FPGA based designs are preferred. From a design perspective, systems built from programmable cores reduce product development and test cycles and are flexible enough to adapt to scenarios in wireless communication system design.

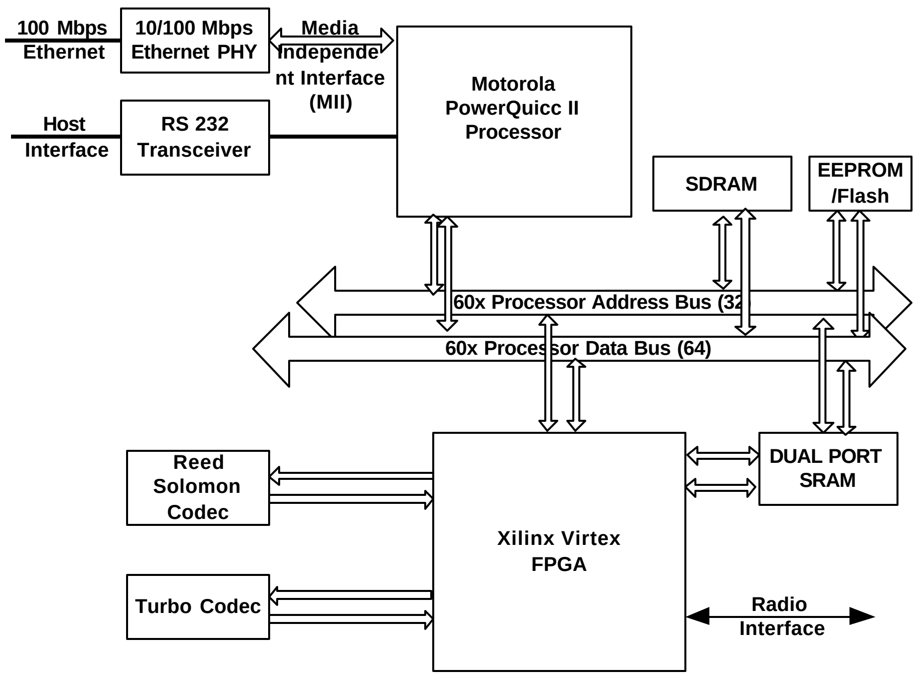

Figure 4 Board Level Design of the Prototyping Platform

The proposed gateway architecture shown in Figure 4 combines the high-performance of a specialized Motorola Communications Processor platform [5] (*PowerQuicc II - MPC8255*) and the flexibility of a high density Xilinx Virtex FPGA [6]. The use of the communications processor simplifies the network interface and host system interfaces. The high density Xilinx Virtex FPGA provides a maximum of 512 I/Os and up to 16 KB of internal static RAM. The available embedded memory can be used to implement the Memory units between processing stages. This provides a highly flexible architecture allowing for evolving or changing standards and protocols. The board level design of the Gateway is shown in Figure 3.

A Board Support Package (BSP) and API developed for VxWorks[2] RTOS can then be used to develop the application software.

V. Acknowledgements

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