LA-UR- 02-3081

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Title:

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Submitted to:

Military and Aerospace Applications of Programmable Logic Devices (MAPLD)
Laurel MD, USA September 2002

Los Alamos
NATIONAL LABORATORY

Reliability of Programmable Input/Output Pins in the Presence of Configuration Upsets

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Abstract

Field programmable gate arrays (FPGAs) are an attractive hardware design option for space based applications because of their in system re-programmability. As opposed to application-specific integrated circuits (ASICs), FPGAs can be configured and reprogrammed while the spacecraft is in orbit. Such reconfiguration can be used to modify the function of the circuit or adapt to changing mission needs.

While FPGAs offer several advantages for space-based computing, FPGAs are sensitive to radiation effects. In particular, radiation effect can cause single-event upsets (SEUs) within any flip-flop or memory cell within the device. Single-event upsets are especially troublesome when they occur in the configuration memory of the programmable device. The configuration memory of an FPGA defines the routing, logic function, and operating modes of the programmable logic. Upsets in the configuration memory may *change* the operation of the circuit. To operate properly in space, FPGAs must anticpate and mitigate against configuration memory SEUs.

It is especially important to insure that the programmable I/O pins (IOBs) operate correctly in the presence of configuration SEUs. A potentially dangerous situation can result if an SEU alters the functionality of a programmable IOB. For example, a series of SEUs may change the functionality of a programmable IOB from an input into an output. The modified output IOB may cause unanticipated contention on a system bus. Such contention will likely have an adverse effect on the overall behavior of the digital system.

This paper investigates the susceptibility of programmable IOBs to configuration memory upsets. Specifically, this paper will investigate the IOBs on the Xilinx Virtex architecture used within the Los Alamos National Laboratory Cibola flight experiment. This paper will identify the configuration upsets required to change an input IOB to an output IOB (and vice-versa) and a tristate IOB to an always-on output IOB (and vice-versa). Further, this paper will propose a several techniques for improving the reliability of Virtex IOBs in the presence of configuration SEUs.

Test Methodology

The primary purpose of this work is to determine the robustness of programmable IOBs in the presence of configuration memory SEUs. A configuration memory SEU testbed was used to artifically corrupt configuration bits on the Virtex FPGA[1]. Based on the SLAAC-1V FPGA computing board developed at USC-ISI[2], this testbed contains an FPGA configuration controller (PE0) and two FPGAs for configuration memory testing (PE1 and PE2). The SEU testbed operates by intentionally modifying bits within the configuration memory to simulate the presence of configuration SEUs. The behavior of the circuit is closely watched during configuration to determine the effects of configuration upsets on the circuit operation.

The SLAAC-1V testbed was used to investigate the reliability of user programmable IOBs in the presence of configuration upsets. The organization of this IOB test is shown in Figure 1. For this test, a programmable I/O block is configured on both the PE0 and PE1 FPGAs. These two I/O blocks are connected to each other by a signal trace on the SLAAC-1V board. The IOB in PE1 is configured as an input and under normal circumstances will not drive the external wire. The IOB in PE0 is also configured as an input. This IOB, however, includes a weak pull-up resistor. Under normal operation, no IOB drives the external signal and the pull-up drives the signal value high. The value of this signal is registered within PE0 and available to the SLAAC-1V host.

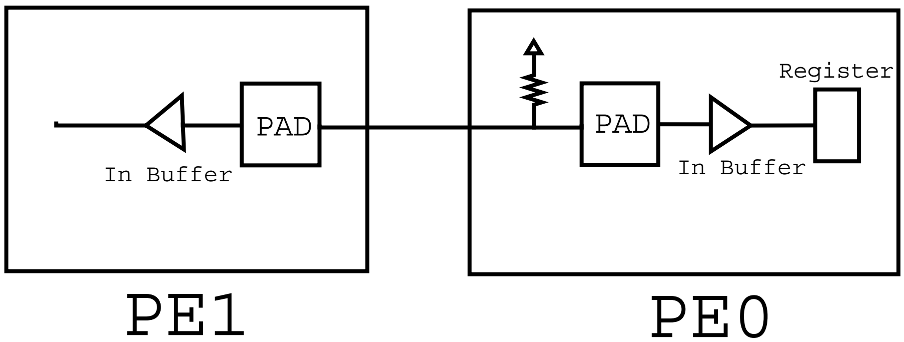

Figure 1: Programmable I/O Test Architecture

The goal of this test is to determine which bits within the bitstream will modify the behavior of the IOB in the PE1. The SEU testbed will intentionally modify the configuration bits associated with the IOB in PE1 and read the contents of the register in PE0. If configuration upsets for the IOB in PE1 change the behavior of the IOB from an input to an output, PE1 will drive a low value on the shared wire and overcome the pullup provided by PE0. A low value on this wire is observable from the host by reading the appropriate register.

For the first test, all single bit changes in the bitstream associated with PE1 are made (there are 54x18 or 972 bits associated with each IOB). After PE1 is reconfigured with a the modified bitstream, the register in PE0 is read by the host to determine if the IOB in PE1 has changed from an input to an output. Based on the results of this test, no single bit configuration upsets were found to change the behavior of this IOB from an input to an output. This result suggests that input IOBs are immune to single-bit configuration upsets.

For the second test, all two-bit combinations of the IOB bitstream are modified (i.e. 972x971 or 471906 two-bit combinations). Again, the value of the PE0 register is read after each two-bit configuration upset to determine the IOB behavior. In this test, ten two-bit combinations bitstream upsets were found to change an input IOB into an output IOB (.002% of the 471906 possibilities). While the IOB is not immune to two-bit configuration bitstream upsets, there is a very small set of configuration bits that will change an IOB into an output. If configuration upsets are distributed uniformly over all bits within the 5,962,944 bit bitstream, the probability that two configuration memory upsets will change an input into an output is 1.44×10^{-10}.

The tests reported above investigate the ability of an input IOBs to be changed into an output IOB. Additional IOB mode changes are also of interest. Specifically, additional tests investigate the ability of an IOB to change from the following modes: tri-state, input, output, and unused. By understanding the reliability of programmable input/output pins in the presence of configuration memory upsets, mitigation techniques can be devised to improve the robustness of FPGA I/O. This work will identify and describe several techniques for increasing the robustness of programmable I/O. Ensuring that IOBs can be made to be immune to configuration error due to SEUs is essential if they are to have a future in space-based applications.

References

[1] Eric Johnson, Michael J. Wirthlin, and Michael Caffrey. Single-event upset simulation on an FPGA. In *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*. CSREA Press, June 2002. To be published.

[2] USC-ISI East. *SLAAC-1V User VHDL Guide*, October 1, 2000. Release 0.3.1.