

# Improving Detectability of Resistive Open Defects in FPGA

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## Abstract

*This paper presents a new technique for detecting resistive open defects in FPGAs. This technique is based on the reconfigurability feature of FPGAs. Using this technique, the detectability of the defect can be improved by several orders of magnitude. Also, a method is developed to scale the detectability. Simulation results show the effectiveness of this method.*

## 1. Introduction

In deep sub-micron technology, opens are the major type of defects. As reported in [Needham 98], it is suspected 58% of return parts have open defects. Unlike an ASIC, most of the area of an FPGA is dedicated to the routing resources and wires of different lengths, hence, open defects are more probable. Most of the customer-returned FPGAs are detected as having open defects. A resistive open is a failure mode in which the connection between two circuit nodes is resistive, where as in defect-free mode it should be completely connected. Resistive open defects increase circuit delay and introduce timing defects in the circuit [Li 01]. For large value of the defect resistance, they even cause hard failures.

The FPGA model we use in this paper is a two dimensional array of *configurable logic blocks* (CLBs) consisting of logic blocks and switch matrices. CLBs are connected through horizontal and vertical wiring channels of different lengths, called *line segments*. There are some *programmable interconnect points* (PIPs) inside each switch matrix that are pass transistors controllable by user-programmable SRAM cells. These PIPs provide selective connectivity between pairs of line segments connected to the switch matrix [Xilinx 02].

In this paper, we address the problem of resistive open defects in FPGAs and present new techniques to detect these defects. Due to the regular structure of the FPGA, we can easily repeat the portion of configuration for one block, developed by our technique, over the whole FPGA to obtain the complete test configuration. Although our technique is primarily developed for application-independent (manufacturing) testing of FPGAs, it can be used for application-dependent testing as well.

## 2. Modeling of Resistive Opens

We use the *delay ratio* as a metric for detectability of resistive open defects, which is defined as the ratio of the delay of defective circuit over that for the defect-free circuit. Larger values of delay ratio indicate better detectability resolution [Li 01][Chang 98a].

The delay of an inverter, as shown in fig. 1.b, can be modeled as  $delay \cong [R_{tr}(V_{DD}) + R_{def}] \times C$ , where  $R_{tr}$  is the transistor turn-on resistance as a function of the supply voltage ( $V_{DD}$ ),  $C$  is the total load capacitance including both gate and wire capacitances, and  $R_{def}$  is defect resistance. As the load capacitance is an unchangeable parameter in ASICs (because the circuit is fixed), traditional methods try to increase the delay ratio by changing the other parameters like supply voltage and test temperature[Baker 99] [Needham 98] [Landolt 96] [Chang 98a] [Chang 98b] [Hawkins

94] [Singh 95]. The improvement in the delay ratio is less than 20% in all these methods [Li 01].

Our technique based on the reconfigurability feature of FPGAs, attempts to change the load capacitance to increase the delay ratio.

### 3. New Technique

In this technique, an additional fanout branch is added to the original path in the configuration, causing considerable increase in delay ratio (up to an order of magnitude). The additional branch is added by activating (turning on) an unused PIP connected on one end to some point in the *Wire Under Test* (WUT). Figure 1.a shows an original configuration for a portion of a WUT, and the simplified transistor-level model is shown in fig. 1.b.

In fig. 2.a, an additional fanout branch is added to point A, and the equivalent effect on the transistor-level model is shown in Fig. 2.b. As we can see in this circuit model, this additional branch is not isolated from the original path, therefore the capacitance of this additional transistor can contribute to the total capacitance seen in the original path, increasing the total delay of the original path.

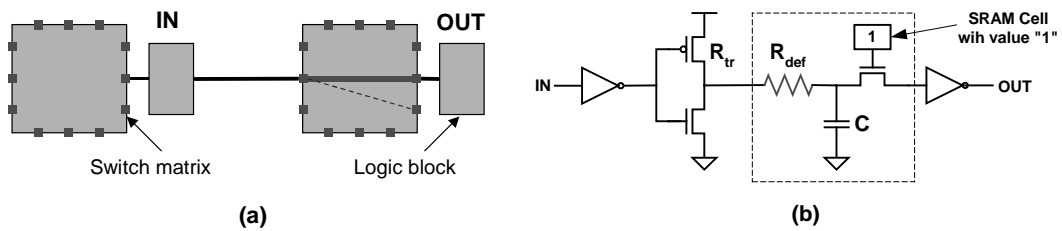


Figure 1 (a) The original configuration for a portion of an FPGA (b) equivalent transistor-level model

This technique is scalable, in the sense that we can add more fanout branches to this path, up to the number of PIPs connected to the point A in fig. 2.a. The increase in delay of the original path is approximately proportional to the number of fanout branches added to the configuration.

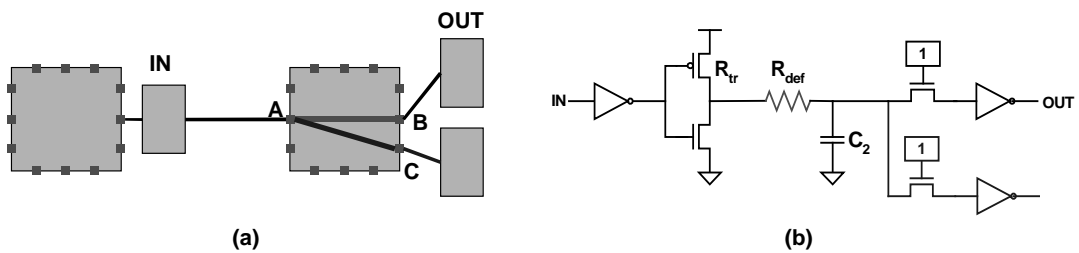


Figure 2 (a) New configuration with additional fanout (b) equivalent transistor-level model

### 4. Simulation Results

We performed SPICE simulation for the circuit model of fig. 2.b. The effect of adding fanouts to the original WUT on the delay ratio is shown in fig. 3. The increase in the delay ratio is almost proportional to the number of added fanouts.

We also performed some simulations to study the effect of path length on the delay ratio. We considered a routing path of different lengths (different numbers of PIPs in the path). We studied two different cases, namely buffered PIPs and unbuffered PIPs. In

both cases, we studied the worst case analysis, meaning we added only one fanout branch to the first PIP in the path and considered the effect of path length on delay ratio. The improvement in delay ratio is almost unchanged when the path length increases - our technique is relatively insensitive to path length.

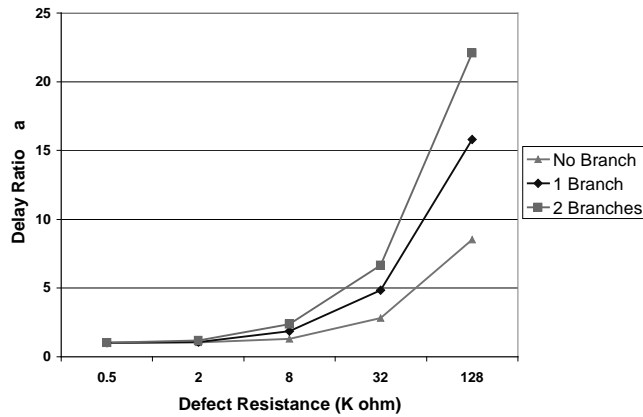


Figure 3 Delay ratio for additional branches

## 5. Summary

In this paper, we presented a new technique to improve detectability of resistive open defects by adding additional fanouts to the original path in order to increase the load capacitance, thus increasing the delay ratio. We performed SPICE simulations to show its effectiveness. The presented technique can be used for both manufacturing test and yield enhancement procedures, and application-dependent testing of FPGAs.

## References

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