

Single-Event Upset Susceptibility Testing of the Xilinx Virtex II FPGA

Gary Swift¹, Candice Yui¹, and Carl Carmichael²

¹ Jet Propulsion Laboratory / California Institute of Technology, Pasadena, CA
² Xilinx, Inc., San Jose, CA

The Xilinx Virtex II FPGA is an advanced SRAM-configured, high gate- and pin-count device of current interest to designers, including those dealing with spacecraft and avionics. Previously at MAPLD, results have been presented on earlier families of Xilinx FPGAs which have shown their sensitivity to upset of both the configuration and the user-incorporated memory elements when irradiated with heavy ions and protons meant to simulate the space radiation environment. Thus, a testbed for SEU susceptibility measurements on the XQ2V1000FG256 has been developed and heavy ion test runs have been conducted at the Texas A&M Cyclotron on that bulk-CMOS device in anticipation of the imminent release of the epitaxial version, the XQR2V1000, 3000 and 6000. Demonstration results for “static” configuration upsets are complete and dynamic testing capabilities are currently being incorporated and tested in beam. The dynamic testing is being expanded to measure the effectiveness of upset mitigation techniques, including configuration monitoring and scrubbing and TMR (triple modular redundancy). Results for the XQ device and, if released, the XQR device will be presented, including the two SEFI (single event functional interrupt) modes identified.