

## **Easily Designed ASICs for Flip Chip Applications**

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The technology to be presented by Clear Logic produces ASICs that have several unique capabilities that make them ideal candidates for military and aerospace applications. First, by implementing a coarse-grained architecture that has resources that map to commercially available FPGAs, customers can use an FPGA design methodology rather than the more expensive and engineering intensive ASIC design methodology. Secondly, the ASICs require only a single mask step for customization. This allows for very low tooling costs and short lead times. A third key feature is that built-in test circuitry ( BIST ) together with proprietary automated test pattern generating ( ATPG ) software guarantees 100% stuck at fault coverage for every design with no engineering input from the designers. The advanced test technology provides known good die (KGD) by probing only twelve signal pins plus power and ground on devices that have in excess of 200 I/Os. Thus, the KGD devices are ideally suited for flip chip bonding because of their bonding pad integrity.

The technical details of these features will be covered in the paper.

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