

ADAPTIVE COMPUTING ENABLES HIGH PERFORMANCE AND LOW POWER CONSUMPTION IN NEXT-GENERATION MOBILE AND WIRELESS SYSTEMS

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ABSTRACT

The ever increasing demand for increased mobility in computing systems introduces several physical requirements (e.g., longer battery life, reduced size, lighter weight, etc.), as well as requirements for massive processing power gains. Additionally, there is an increasing expectation for multifunctionality in a single mobile system, including software-defined radio (SDR) capability for globally linking to data and systems. This demanding criteria creates a complex design problem that is compounded by the explicit requirements for high performance and extremely low power consumption.

Furthermore, mobile and/or wireless systems are at the point in the development roadmap where, without a paradigm shift in the basic IC architecture that moves away from fixed-function silicon technology (e.g. ASICs, microprocessors, FPGAs, DSPs), they are not able to meet this demanding criteria for quite some time.

The ideal solution would be to take advantage of the processing power of the ASIC while retaining the flexibility of the DSP. This is the very essence of adaptive computing and its first incarnation in Adaptive Computing Machine (ACM), a new class of IC based on standard CMOS silicon, and described in this paper.

Another design consideration is that developers today have been using FPGA-based reconfigurable computing in a variety of high performance applications. However, FPGA-based technologies are power hungry and only appropriate for wall-socket applications where power consumption is not a constraint, such as base stations and supercomputing. In contrast, adaptive computing presents a new architecture that is not FPGA-based and that offers a highly efficient and adaptable form of computing that results in lower power consumption, reduced silicon area, and higher performance – the needed attributes more next-generation mobile wireless systems.

The performance of an ACM for is validated in hardware through the implementation of a series of baseband algorithms. Benchmarks of the ACM' test chip performance are presented, showing significant improvements to be feasible relative to conventional IC technologies. These benchmarks are based on a real-time demonstration that exemplifies a software programmable IC (the ACM) outperforming a hardwired custom ASIC.

In the paper, the following are discussed:

- Current fixed-function IC implementations – their advantages and limitations for next-generation mobile and/or wireless systems
- Detailed comparison of adaptive computing to reconfigurable computing – issues for low power consumption and general design issues, such as interconnects and capacitance
- Unique aspects of the ACM architecture that enable higher performance, lower power consumption, and greater flexibility as compared to conventional IC technologies
- How an adaptive computing approach addresses current mobile and wireless adversities by enabling the following:
 - The ACM to perform like an ASIC, at the speed of an ASIC, but programmed by means of software – *dynamically configured at run time*.
 - Full system scalability
 - Micro and macro levels of adaptability
- The spatial and temporal segmentation (SATS) process of the ACM that enables multifunctionality and SDR to occur at low power consumption. Unlike conventional IC technologies, the ACM architecture adapts to the problem at hand, enabling timesharing, or spatial and temporal segmentation. SATS is the process of mapping algorithms for a given task to dynamic hardware resources, then rapidly performing various portions of an algorithm in different segments of time (temporal) and in different locations in the adaptive fabric (spatial) of the ACM. With SATS, the ACM's gates are rapidly reused, bringing into existence for the exact amount of time needed -- clock cycle by clock cycle -- the hardware an algorithm requires, and then efficiently running any number of different algorithms on the hardware engine.
- ACM performance example: Benchmarks for the ACM test chip are based on two key wireless standards, cdma2000 and WCDMA. The benchmark elements are selected for their emphasis on compute-intensive operations that are historically done in ASICs, and for comparing an ACM to the known high-performance, fixed function ASIC solution.