

Title: A Reconfigurable 1.5 GB Stacked SDRAM Board

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Abstract

Recent advances in technology, specifically high speed FPGA and stacked SDRAM, have made it possible to develop large memory boards for space applications. The NASA GIFTS, Geostationary Imaging Fourier Transform Spectrometer, is a space application for such a system. The GIFTS satellite will require a reconfigurable memory board to act as a large circular buffer as well as a “standard” memory subsystem. The board is being designed for a seven year mission requiring 100 KRad total dose to support the geosynchronous orbit. The single event requirements for the system require on board EDAC (Error Detection and Correction) for reliable operation. A 6U form factor will be used. The board will have a Compact PCI interface with block DMA transfer capability using Actel’s PCI core technology. Additionally the system will have LVDS (Low Voltage Differential Signaling) for high-speed data transfer to the memories. The board can be configured in two operational modes; read/write mode and buffer mode, refer to the Figure 1 below.

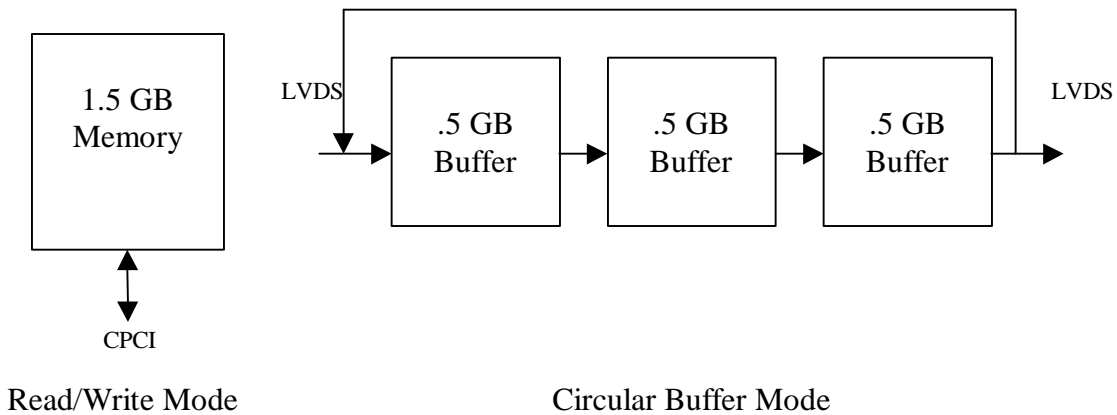


Figure 1. Operational Modes

A block diagram of the memory system is given in Figure 2. Control, data path modules and the SDRAM controllers are to be implemented in the Actel 54SX RadTolerant FPGA. The current plan is to use 2Gbit SDRAMs and Serialized/Deserialized LVDS interfaces.

The command and configuration module combined with the mode control module will determine to operational mode of the system. The CPCI interface has been prototyped and is operational. A prototype of the LVDS interface is underway. The completed board design is planned for March 2002. The completed system will support 1.5 Gbytes of error corrected memory for CPCI-based systems.

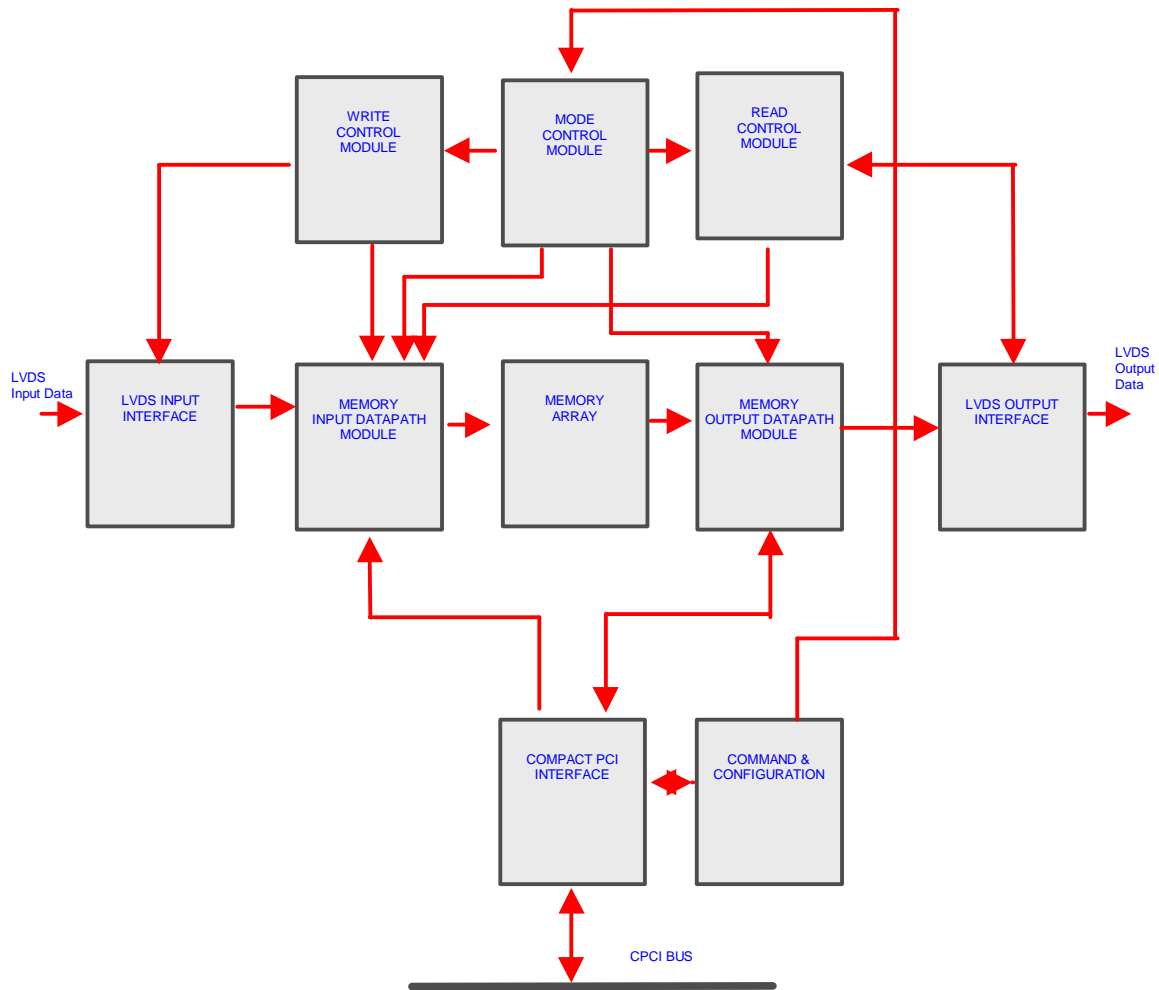


Figure 2. Memory Board Block Diagram.