

Implementation Trade-offs of Triple-DES in the SRC Reconfigurable Computing Environment

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The SRC Computing Environment has a hybrid architecture, which employs both general-purpose high-performance microprocessors and reconfigurable processor chips. The SRC-6E system consists of Intel® PIII 1.0 GHz processors running the Linux operating system. Attached to these microprocessors are two SRC Multi-Adaptive Processors (MAPTM). Each MAP board consists of two Xilinx® VirtexII XC2V6000 FPGA chips in addition to a control processor. It is the MAP components that the MAP compiler targets. All code that is run on the Intel processor is compiled separately. SRC has a rich programming interface, which enables several alternatives for application implementations. In this paper, we overview the architecture and programming model for the SRC and study, using Triple-DES cryptography application, the trade-offs associated with the different possible implementations. Using SRC high level programming interface we will particularly show that the underlying model allows the programmer to easily manage the tradeoffs between chip area versus design speed. Impact of this high-level programming environment on time-to-solution as well as ease of use and level of hardware design knowledge for application developers will be assessed.