



A Fast Transform DSP Coprocessor

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Abstract

Satellite on-board data processing capability has been greatly improved with the availability of a space qualified 32-bit floating point DSP, the TSC21020F. Although the performance of 40 Mflops at 20 MHz clock frequency is sufficient for a large number of on-board processing tasks, applications based on high throughput FFTs and filtering calculations would still require the use of many DSPs operating in parallel. An assessment of existing and planned mission requirements indicates that up to 20 DSPs could be required to satisfy the performance requirements of these applications.

While it is technically no problem to implement such a system of parallel DSPs, restrictions in budgets (mass and power) generally prohibit the use of those parallel processing systems in scientific or commercial satellites.

In order to solve that problem, the development of a coprocessor for a DSP specifically suited for these application demands has been undertaken by the European Space Agency in conjunction with European Industry. This effort results in a Fast Transform Coprocessor (FTC), which is not only specialised in performing FFTs, but general transforms such as wavelets and filters.

The improvement by using such a dedicated co-processor could be as high as 25 times the performance of a DSP alone. This is particularly true for small block size FFT's, FIR filters and possibly other very basic transforms in general. For example, the on-board processing of one 100km ENVISAT – ASAR type scanSAR swath of a future SAR instrument would be achievable with a single processing module comprising one DSP and one FTC, instead of five standard DSP-modules containing just a DSP. The DSP TSC21020F, as a universal programmable device, provides the flexibility, whereas the FTC as a simple programmable device provides the speed. The combination in one module provides high performance and flexibility adaptable to a wide range of applications: SARs, scatterometers, altimeters, spectrometers, and interferometers.



The FTC device is supported by external address generators, implemented in FPGAs and a range of external memory banks. The latter can be, depending on the application needs, EDAC protected to prevent radiation-induced bit errors corrupting the data.

The paper will present the architecture and the implementation of the DSP coprocessor. The architecture and implementation of a demonstrator unit, comprising a combination of a TSC21020F DSP and the coprocessor, will also be presented in detail, as well as the different operation modes of the system.

A summary of the experiences gained with the system will round off the paper and the presentation.