

# SEU and SET Mitigation Techniques for FPGA Circuit and Configuration Bit Storage Design

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## Abstract

A unique hardening technique is described which addresses SEE (Single Event Effect) problems which result in data loss in deep submicron microcircuits in space radiation environments. This hardening technique, termed the "temporally redundant sampling latch", addresses both conventional static SEUs (Single Event Upsets) and SET (Single Event Transient) induced errors. The temporal latch approach provides immunity to each of these SEE related circuit upsets with a minimal impact on microcircuit design methods, physical layout area, and circuit performance. For FPGA (Field Programmable Gate Array) designs in particular, the layout area penalty and the circuit operation speed are impacted by only a few percent. The temporally redundant latch approach therefore permits FPGAs and other microcircuits with deep submicron feature sizes to be used in space environments. It not only eliminates single event upsets, but also prevents single event transients, generated within combinatorial logic or within EEPROM (Electrically Erasable Programmable Read-Only Memory) configuration bit storage elements, from disrupting the circuit operation.

## I. INTRODUCTION

As the microelectronics industry has advanced, IC designs in general and FPGA designs in particular have experienced dramatic increases in both density and speed largely due to decreasing feature sizes with which these devices can be manufactured. These advances are not without serious implications for microelectronics used in space applications where ICs are subjected to total ionizing dose as well as single event effects. Of these effects, single event upsets represent the radiation-induced hazard most difficult to avoid in spaceborne microelectronics systems.

In describing SEE mitigation techniques, we consider CMOS device technologies and their response to the cosmic ray environment of space. In particular, we address the following issues:

- (1) the impact that shrinking device sizes has on SEUs in spaceborne FPGAs due to the cosmic ray environment;
- (2) the importance of SETs in the combinatorial logic of FPGAs with feature sizes smaller than 0.35 micron; and
- (3) the importance of SETs in EEPROM configuration bits of FPGA with features sizes smaller than 1.0 micron.

We first review upset effects and their mechanisms and describe the implications for present day spaceborne

FPGAs. We distinguish between two distinct upset mechanisms. The traditional SEU mechanism is related to logic state changes in storage cells (flip-flops, memories, latches, etc). An emerging upset mechanism known as SET begins to impact the operation of space systems fabricated in deep submicron CMOS and submicron EEPROM technologies. Several conventional and commonly used SEU and SET mitigation techniques are then discussed along with their inherent limitations. Finally, we describe a new and novel circuit approach that is inherently immune at any technology feature size to both present day upset mechanisms and to emerging upset mechanisms. This new approach is termed either the "temporal sampling latch" or the temporally redundant latch". It not only addresses upsets in latches, but also addresses upsets caused by transients in combinatorial logic, global clock signals, and global control lines. When applied with special latches, the approach can also eliminate upsets caused by a single cosmic ray simultaneously striking two sensitive junctions.

## II. SINGLE EVENT UPSETS AND SINGLE EVENT TRANSIENTS

### A. Shrinking Size and SEE Related Upsets

The effects of scaling on the single event response of microelectronics are a direct result of the physics of energy loss, charge collection, and upset due to a cosmic ray striking a junction in an IC device. The review here is brief and qualitative. Many good summaries exist [1], [2], [3] that review these concepts in more detail.

When an energetic ion passes through any material it loses energy through interactions with the bound electrons, causing an ionization of the material and the formation of a dense track of electron-hole pairs. The rate at which the ion loses energy is the stopping power ( $dE/dx$ ). The incremental energy  $dE$  is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units of  $mg/cm^2$ . The radiation effects community has adopted the term LET (Linear Energy Transfer) for the stopping power. An ion with an LET of  $100 MeV\cdot cm^2/mg$  deposits approximately 1 pC of electron-hole pairs along each micron of its track through silicon.

In the presence of electric fields, these electron-hole pairs quickly separate as they drift in opposite directions in the field and are quickly collected by whatever voltage sources are responsible for the field, thus producing a current transient. In bulk CMOS designs, such electric

fields are present across every pn junction in the device. If an ion strikes a junction connected to a signal node, a current transient is subsequently observed on the signal node as the electric fields in the junction and funnel regions separate the electron and hole carriers. The initial prompt current pulse is short lived, lasting on the order of only 100 to 200 picoseconds.

High energy protons and neutrons are also known to produce similar effects indirectly through nuclear reactions within the silicon. In these cases, a heavy ion recoil reaction byproduct passes through a junction and produces a similar charge collection current pulse. In space, high energy protons primarily originate from the trapped proton radiation belts and from solar flares. For high-altitude aircraft, both high energy neutrons and protons are encountered as reaction byproducts found in cosmic ray showers formed when an energetic heavy ion from space undergoes a nuclear reaction in the atmosphere.

These induced currents are responsible for SEUs observed in spaceborne circuits, typically static latches and SRAMs (Static Random Access Memories), over the last 10-15 years [4]. The effect that these currents have on a circuit depends on the response of the circuit to the charge collected on the signal node. Basically, the capacitance of the signal node (to first order) determines how large a voltage swing  $dV$  results from the collection of a charge  $dQ$  according to  $dV=dQ/C$ . For latches and SRAMs, positive gain feedback loops cause a data bit flip once the collected charge reaches a critical value ( $Q_{crit}$ ) sufficient to drive a node voltage past the switching voltage.

SEU in static latches and SRAMs became an important issue once feature sizes dropped below 10 microns and the critical charge for upsetting a circuit dropped below 1 pC (roughly corresponding to a particle LET of 50 MeV  $cm^2/mg$  and a collection depth of 2 microns). Static latch SEU vulnerability has been calculated [5] and measured [3] as a function of technology feature size to establish the relationship between the critical charge needed to upset the circuit and the technology feature size. All results indicate that the critical charge needed to upset a latch decreases as the square of the feature size. If this relation holds as electronics feature sizes decrease from 0.8 micron (present day spaceborne) to 0.18 micron (present day commercial), the critical charge decreases by nearly a factor of 20.

Experimentally observed LETs for 0.8 micron standard cell latch designs have been as low as 5 MeV- $cm^2/mg$  and as high as 20 MeV- $cm^2/mg$ . Even with thinner epi layers, 0.18 micron designs could have SEU threshold LETs no higher than 1 MeV- $cm^2/mg$ . While the area cross section for a heavy ion hit is be a factor of 20 lower, the integral fluency of cosmic rays above 1 MeV- $cm^2/mg$  is 1000 times larger than the fluency above 20 MeV- $cm^2/mg$  for a geosynchronous orbit [1]. This implies an SEU error rate (per bit) increase of a factor of 50. Since 0.18 micron designs typically have 20 times the number of latches on a given die size as 0.8 micron designs, the total IC error rate is

1000 times larger. Clearly novel approaches are needed to alleviate the problem.

## B. An Emerging Upset Mechanism

Cosmic rays can also induce transients in combinatorial logic, in global clock lines, and in global control lines. These single event transients, or SETs, have only minor effects in present 0.8 to 0.5 micron technologies since the speed of these circuits is insufficient to propagate the 100 to 200 ps SET any appreciable distance through the circuit. However, as smaller feature size (and thus faster) technologies find their way into spaceborne systems, these transients become indistinguishable from normal circuit signals.

Nonvolatile and reconfigurable FPGAs, such as that described in Reference [6], use EEPROM transistor circuits for configuration storage. Single-event simulations of these EEPROM storage cells indicate relatively long recovery times approaching 1000 ps. This time is long compared to the response time of the CMOS logic and routing switches in the 0.8 micron technology in which the device is fabricated. As a result, cosmic ray events in the EEPROM cells might temporarily alter the logic element lookup table function or alter the routing interconnect for a sufficiently long time that the resulting signal glitch propagates through the entire FPGA just as a normal signal. It should be noted that slow recovery time is a general property of any circuit that uses EEPROM devices in an active fashion. The programmed threshold voltage of EEPROM devices is simply not large enough to provide charge dissipation drives comparable to normal CMOS.

This is illustrated in Figure 1 which shows, as a function of technology feature size, the critical transient pulse width needed in order to propagate without attenuation through an infinitely long chain of inverters. At pulse widths smaller than the critical width, the inherent inertial delay of the gate causes the transient to be attenuated and the pulse, after passing a few gates, dies out. At pulse widths equal to or larger than the critical width, the transient propagates through the gate just as though it were a normal circuit signal. As a general rule of thumb, transients of width greater than the critical width propagate through any number of gates without attenuation, transients of width less than half the critical width terminate in the first gate, and transients of intermediate width propagate through a varying number of stages.

The curve in Figure 1 is the result of SPICE [7] simulations performed for various technology feature sizes (shown by the dots on the curve) between 1.2 microns (1200 nm) and 0.13 microns (130 nm). A generic set of SPICE model parameters was developed using known model parameters for technology sizes between 1.2 microns and 0.7 microns, inclusive. The constant field scaling rules were applied to the generic model and to the transistor sizes to predict model parameters at the smaller feature sizes. Our scaled values of various critical parameters ( $V_{DD}$ ,  $V_{TH}$ , and  $T_{OX}$ ) were consistent throughout with projections

published in the National Technology Roadmap for Semiconductors [8]. The solid curve in Figure 1 simply connects the simulation points while the dashed curve simply extrapolates the points to 0.05 micron (50 nm), the projected feature size of commercial technologies in the year 2012.

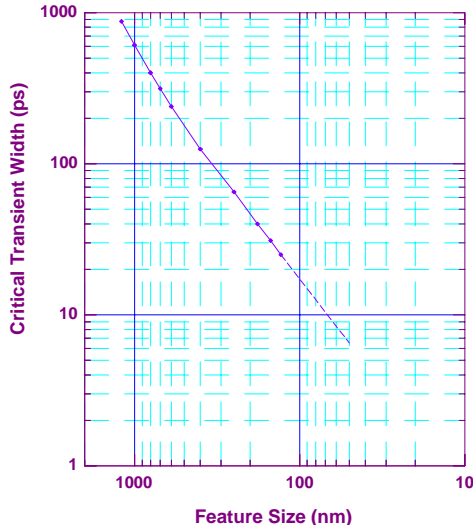


Figure 1. Critical Transient Width Versus Feature Size for Unattenuated Propagation.

As discussed earlier, cosmic ray induced CMOS transients have pulse widths of 100 to 200 ps while EEPROM transients have widths an order of magnitude larger. Thus, for FPGAs fabricated with feature sizes smaller than 0.35 microns, CMOS induced SETs are no longer be attenuated within the gates of the device and therefore propagate as normal circuit signals. Similar SET propagation occurs for EEPROM induced SETs in FPGAs fabricated with feature sizes below 1.0 micron.

Figure 2 illustrates the circuit topology found in all sequential circuits. In FPGAs, the sequential circuitry represents the routing switches and logic elements that precede each D-Flip-Flop on the chip. The data from the first latch (U1) is typically released to the combinatorial logic on a clock edge, at which time logic operations are performed gates. The output of the combinatorial logic reaches the second latch (U2) sometime before the next clock edge. At this clock edge, whatever data happens to be present at its input (and meeting the setup and hold times) is stored within the latch.

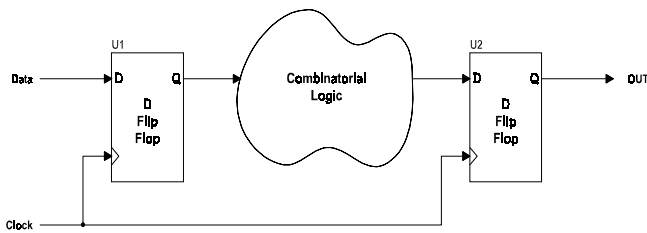


Figure 2. Typical Sequential Circuit Topology.

If a heavy ion strike occurs within the combinatorial logic block, and the logic is fast enough to propagate the induced transient, then the SET eventually appears at the input of the second latch in Figure 2 where it may be interpreted as a valid signal. Whether or not the SET gets stored as real data depends on the temporal relationship between its arrival time and the latching edge of the clock. Additional invalid transients can occur at the combinatorial logic outputs as a result of SETs generated within the signal lines that control the function of the logic. An example of this is an SET generated within the configuration storage circuitry that controls either the FPGA logic functionality or the routing connectivity.

This is illustrated in Figure 3 for the case that the true data is low and a positive SET appears at the input to the latch. The transient is incorrectly interpreted as valid data, and subsequently stored in the latch, if it is high from a setup time before the clock edge to a hold time after the clock edge. The figure shows four times at which an SET can arrive, with (a) and (d) satisfying a non-latching condition and (b) and (c) satisfying the earliest and latest, respectively, arrival times for a latching condition. Similar errors can occur from transients that might appear on the clock line. References [9] and [10] give several examples of clock SET induced errors.

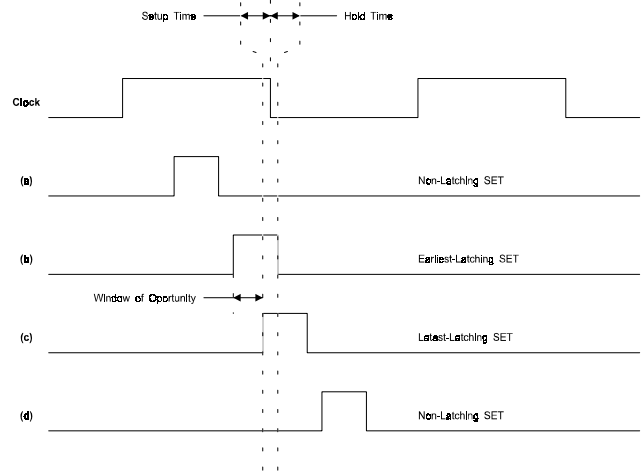


Figure 3. Temporal Relationship for Latching a Data SET as an Error.

The radiation-effects community is becoming aware of the problem and the propagation of SETs has recently been investigated [11] as part of an effort to develop software for estimating error rates in complex VLSI (Very Large Scale Integration) designs. The thrust of this effort was to develop algorithms and software, based on experimentally observed transient pulse attenuation through combinatorial gates, to predict SET induced error rates in deep submicron ASICs. Test circuits were fabricated for this effort in a 1.0 micron CMOS process. Pulsed laser illumination of circuit junctions was used to induce transient pulses wide enough to propagate appreciable distances (heavy ion induced pulses are too narrow to produce effects in a 1.0 micron process). It should be noted that the authors observed a

critical transient pulse width (infinite transmission through their inverter chain test circuits) of 680 ps, which compares favorably with 610 ps that we calculate (Figure 1) with our generic scaled SPICE models.

It is also important to note how the various error rates (latch SEU and combinatorial logic SET) in sequential circuits depend on the clock frequency. Upsets can occur in latches only when the clock is low and the latch is in a hold state. Since the clock is always low 50% of the time, latch SEU rates do not depend on the clock frequency. However, SETs produced in the combinatorial logic are stored if they reach the latch input coincident with clock edges, the number of which depends linearly on the frequency. Thus the SEU rate for latches is independent of clock frequency while the combinatorial logic SET error rate is directly proportional to clock frequency. These error rate relations have been demonstrated experimentally [12] using pulsed laser illumination of test circuits while measuring both error rates as a function of frequency. The SET problem is therefore compounded as IC technology feature sizes shrink since smaller feature sizes result in smaller gate delays that permit circuits to be operated at higher clock frequencies. Not only does each combinatorial gate in a circuit contribute transient errors (because transients are no longer be attenuated), but the probability of storing any given error also increases (because of the higher clock frequencies).

It is useful to introduce the concept of an SEU-SET crossover frequency. The crossover frequency is defined as the frequency above which SET induced errors will exceed SEU errors of unhardened latches. Alternatively, at the crossover frequency, hardening the latches in a design will only reduce the device error rate by one-half. A simple calculation shows that the crossover frequency ( $F_{\text{crossover}}$ ) is related to the susceptible areas of both the latches ( $A_{\text{latch}}$ ) and the contributing combinatorial logic ( $A_{\text{combinatorial}}$ ) in the design as well as to the transient pulse width (TW) according to

$$F_{\text{crossover}} = (A_{\text{latch}} / A_{\text{combinatorial}}) / (2 * TW)$$

For CMOS induced transients, this frequency is typically on the order of hundreds of MHz for typical FPGA layouts. For EEPROM induced transients, the crossover frequency can easily be as small as tens of MHz. It is therefore no surprise that present day testing of CMOS FPGA designs, typically limited to frequencies less than 5 MHz [13], have not seen any errors attributable to SETs. Other experiments, based on system-level TMR [14] with no nodes common to any of the three circuits, will also never see SETs (but will suffer from error latency effects in all but the most simple test circuit instantiations).

### III. CONVENTIONAL SEE HARDENING APPROACHES

Several obvious hardening approaches can be used to help mitigate static latch upsets as well as transient pulses in combinatorial logic and clock lines. The most straight

forward approach is to use high drive transistors with increased node capacitance [15]. High drive transistors dissipate the transient charge more quickly and high node capacitance reduces the voltage excursions resulting from the transient charge. This necessarily results in physically larger circuits (for the high drive devices) with longer propagation times (from the capacitance needed to attenuate SETs). These conventional approaches have successfully produced circuits having SEU threshold LETs above 30 MeV-cm<sup>2</sup>/mg for designs fabricated in feature sizes greater than 0.5 micron. The approach is not practical, however, as technology feature sizes reach the deep submicron level since it is nearly impossible to design latches with LETs exceeding 3 to 5 MeV-cm<sup>2</sup>/mg.

Triple module redundancy, or TMR, was first introduced in the 1980s [16]. TMR is a circuit hardening approach, does not rely on any increased capacitance in the layout, and is therefore amenable to deep-submicron designs. Basically, since three redundant latch paths (with common input) are voted on to provide the correct result, the TMR approach does not provide any inherent immunity to errors induced by SETs on either the data input, set and/or reset control lines, or the clock line. Clock SET induced errors are particularly problematic for commercial design approaches where both clock and its complement (both needed for CMOS implementations) are buffered locally within the latch and thus introduce very low capacitance nodes susceptible to SETs at very low LETs.

A newer approach, developed in the early to mid 1990s, effectively replaces TMR with special latches that can only be upset if two critical nodes are simultaneously struck by a heavy ion. The first such latch was developed by Dooley [17] and required four times the number of transistors as a conventional latch. A subsequent design, the DICE (Dual Interlocked CELL) latch [18] only requires twice the number of transistors as a normal latch. Although the original motivation of these designs was the same as TMR (to reduce static latch upset rates), the DICE-based approach can go beyond TMR techniques and also mitigate (albeit with limitations) several SET induced error modes.

The technique of using a DICE-based latch with a separation delay to filter SETs is illustrated in Figure 4. For the latch to change state, both data inputs (D and DP) must be driven. By adding a delay of length TD in one of the data input paths, all data SETs of width TW less than TD are eliminated. The filtering delay necessarily increases the latch setup time by an amount equal to twice the delay time TD. In the absence of single event transients, the latch assumes the correct state after one delay time. In the presence of single event transients, the correct state is not assured until after two delay times. (Exactly the same situation arises for a voting system that uses a majority gate with prompt, single-delayed, and double-delayed inputs. The output is correct after one delay time if no events occur but cannot be assured until two delay times if events are present.)

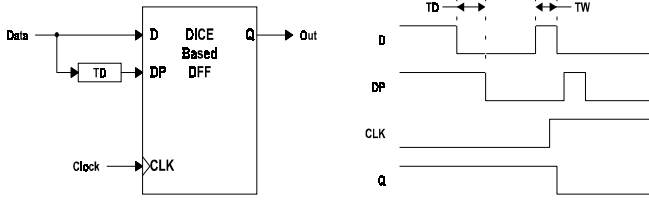


Figure 4. DICE Latch With Separation Delay to Filter SETs.

Another, and even more severe limitation of this method is that for SET widths  $TW$  exceeds  $TD$  by even the smallest amount, all transient immunity is abruptly lost. In our earlier FPGA designs [6], we had previously used DICE-based latches with filtering delays to filter out the relatively long SETs introduced into the device by the EEPROM storage elements. Because of the inherent problems associated with this the technique, special circuit techniques were employed to ensure that the delay  $TD$  was always long enough. These limitations have subsequently been overcome with our newer temporal latch approach which is described below.

Hardening measures could alternatively be taken at the system level. Redundant computation, either using multiple chips or multiple calculations on a single chip, could be used to detect errors. The latency of an error becomes an issue in these cases because it may be many clock cycles before an error manifests itself at the circuit outputs. Should an error be detected, rollback to a previously known good state would have to occur. This approach places a heavy burden on the system engineers and results in overly complex systems that necessarily include both error detection as well as periodic storage of known good state variables so resets can be performed.

#### IV. TEMPORAL LATCH SEE HARDENING SOLUTION

Having identified the problems associated with SEE in deep submicron microcircuits and having described the inherent limitations of conventional mitigation techniques, we now describe a new temporal sampling latch approach [9], [10] that is inherently immune at any technology feature size to both present day upset mechanisms and to emerging upset mechanisms. The intended use of the temporal latch is to replace conventional latches in any sequential circuit that must provide high, or total, immunity to SEU. The new approach not only addresses upsets in latches, but also addresses upsets caused by transients in combinatorial logic, global clock signals, and global control lines. The new approach, when applied with special latches, can also eliminate multiple bit upsets in sequential circuit designs.

##### A. Latch Construction

A simple embodiment of the temporal sampling latch is shown in Figure 5. The circuit contains nine level sensitive latches (U1 through U9), one majority gate (U10), and three inverters (U11 through U13). Each level sensitive latch is transparent (sample mode) when its clock input is high and

is blocking (hold mode) when its clock input is low. When in sample mode, data appearing at the input  $D$  also appears at the output  $Q$ . When in hold mode, the data stored within the latch appears at the output  $Q$  and any data changes at the input  $D$  are blocked. Two level sensitive latches in tandem and clocked by complementary clock signals (such as U1 followed by U2) form an edge triggered D-Flip-Flop. With the clock inversions used in Figure 5, the D-Flip-Flops formed by (U1, U2), (U3, U4), and (U5, U6) are triggered on the falling edges of the clocks  $CLKA$ ,  $CLKB$ , and  $CLKC$ , respectively.

The complement of each clock is formed locally by the inverters U11, U12, and U13. There is no need, for hardening purposes, to route global complimentary clock signals over the chip in order to maintain high capacitance nodes. Heavy ion induced transients on the low capacitance internal clock nodes do not affect the SEU immunity of the temporal sampling latch.

The three D-Flip-Flops (U1, U2), (U3, U4), and (U5, U6) operate in parallel and form the temporal sampling stage of the circuit. Each of these three D-Flip-Flops drives another level sensitive latch. These latches (U7, U8, and U9) together with a simple majority gate (U10) form the sample release stage of the circuit.

The upset immunity of the circuit in Figure 5 is a consequence of two distinct parallelisms: (1) a spatial parallelism resulting from the three parallel circuit branches and (2) a temporal parallelism resulting from the unique clocking scheme. Previous redundant systems have used only spatial parallelism to achieve SEU immunity to cosmic ray strikes in static latches (inherently spatial). Immunity to SETs in combinatorial logic and global clock lines (inherently temporal) cannot be achieved with spatial redundancy alone -- some form of temporal redundancy must be additionally included.

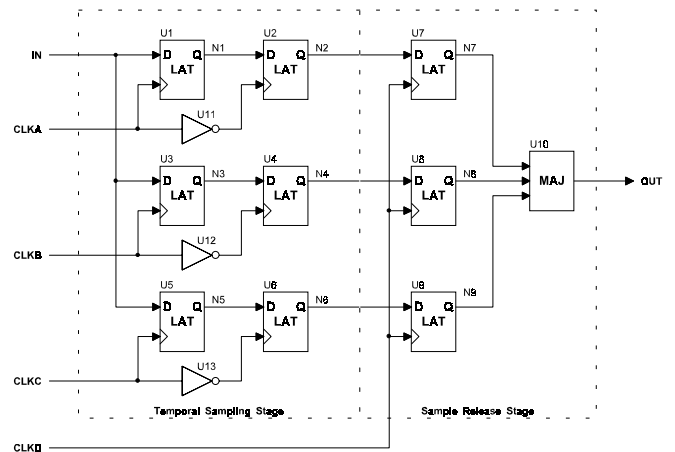


Figure 5. Temporal Sampling Latch With Sample and Release Stages.

Why not just replicate the combinatorial logic and the clock lines to form a totally spatially redundant circuit? This is exactly what has been done for redundant computation described above and error latency becomes a

problem. In our approach, the combinatorial logic is effectively replicated, not in space but in time. The same logic is really just used at three different times. The result of this is that errors are flushed on each clock cycle and the maximum error latency never exceeds a clock period.

Temporal redundancy of our circuit is achieved by combining a temporal sampling stage with a sample release stage where the sampling is controlled by three clocks (CLKA, CLKB, and CLKC) and the release is invoked by CLKD. The clocking scheme is therefore central to the operation of circuit and is now discussed.

## B. Clocking Scheme

The clocking scheme is shown in Figure 6. The figure shows two cycles of the master clock and two cycles of the temporal sampling latch control clocks. The master clock (top curve) would generally be the clock signal brought onto the chip through an input pad. The bottom four curves in Figure 6 show the four clock signals (CLKA, CLKB, CLKC, and CLKD) used above in Figure 5. The CLKB and CLKC widths can be substantially shorter than the CLKA and CLKD widths. Their widths need only be greater than the maximum width of any SET induced in the combinatorial logic. Unlike the DICE-based latch with filtering delay described above, the temporal latch only gradually loses its SET immunity as the transient width TW begins to exceed either the CLKB and CLKC widths.

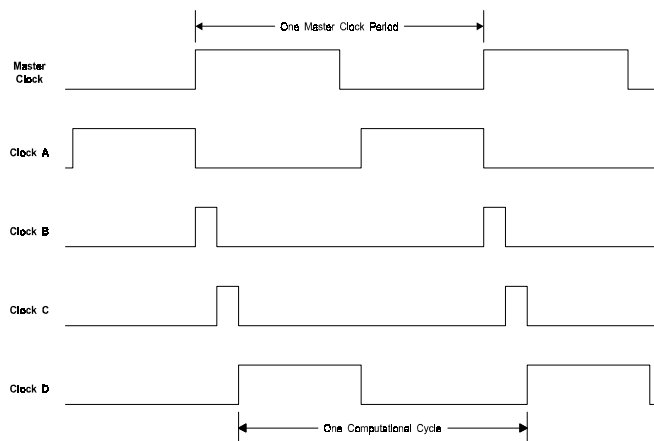


Figure 6. Temporal Latch Control Clocks Derived from Master Clock.

The temporal latch can also operate in a "fast mode" [9], [10] that can be designed to be selectable from an input control signal. In this mode, clock generation circuitry is selected which holds CLKD high so that the sample release stage of each temporal latch is always transparent and the sampling clocks (CLKA, CLKB, and CLKC) are each driven by the master clock signal. Conventional static latch SEU immunity is retained in this mode since we still have three D-Flip-Flops operating in parallel. As in TMR approaches, immunity to data SET induced errors is lost. Unlike TMR approaches, however, immunity to clock and set/reset control line SET induced errors is retained.

The fast mode of operation can be of use for earth-based testing. In such tests, the device is placed in a beam of high-energy heavy ions produced by an accelerator and error rates are measured. By operating the temporal latch in fast mode, error rates due to data SETs alone can be measured as functions of LET and frequency since static latch SEUs are suppressed. Such testing can provide important data to characterize fabrication technologies as a function of feature size.

## C. Circuit Operation

The operation of the circuit of Figure 5 with the clocking sequence of Figure 6 is most easily explained if we start at the beginning of a computational cycle which begins at the rising edge of CLKD. At this time the sample release latches (U7, U8, U9) pass their input data to the majority gate (U10) where it subsequently appears at the output node (OUT). CLKD subsequently goes low, the release latches (U7, U8, U9) enter a hold state, and this original data remains asserted on the output for the remainder of the computational cycle.

This output data is then processed by intervening combinatorial logic before it appears at the input to the next temporal sampling latch. The data must arrive at the input to the next stage before the falling edge of CLKA at which time the data is stored in the a D-Flip-Flop formed by latches U1 and U2. CLKB then goes high to sample the input. Whatever data is at the input when CLKB goes back low is then stored in the D-Flip-Flop formed by latches U3 and U4. Finally, CLKC toggles high and low to sample and hold the input data in the final D-Flip-Flop formed by latches U5 and U6.

At this time another computational cycle begins. The input data to each temporal sampling latch has been asserted on the three inputs to the sample release stage. When this next computational cycle begins, CLKD again goes high and the data appears at the output of the majority gate.

Data is released to the combinatorial logic on each rising edge of CLKD and must reach the next sampling latch before the falling edge of CLKA (minus the setup time). From Figure 6, this is thus the period of the master clock minus the D-Flip-Flop setup time and minus the sum of the CLKB and CLKC durations. An equivalent way of viewing the incurred speed penalty is that the temporal latch setup time is effectively increased by the sum of the widths of the CLKB and CLKC phases.

## D. Elimination of Upsets

Upsets of the temporal sampling latch are avoided as a result of the spatial parallelism provided by the three circuit branches and the temporal parallelism provided by the sampling and release architecture of the design. Space limitations of this paper prohibit us from explaining the temporal latch upset immunity in any great detail. The reader is rather referred to Section VI.D of Reference [9] or to Section 3.4 of Reference [10] which describes the temporal latch upset immunity in terms of each of four

distinct upset mechanisms: (1) static latch SEU, (2) data SET, (3) sampling clock SET, and (4) release clock SET. The first of these, static latch SEU, is the upset mechanism of primary concern in present day spaceborne microelectronics systems fabricated in 0.8 micron to 0.5 micron feature sizes. The last three mechanisms are of concern in systems fabricated in 0.35 micron and smaller feature sizes.

Two critical points are, however, worth reiterating: (1) the temporal latch is totally immune to upset from a single cosmic ray striking a single circuit node, and (2) any cosmic ray induced erroneous data is not only vetoed by the spatial and temporal redundancies, but it is flushed within a single clock cycle.

### *E. Multiple Node Heavy Ion Strikes*

The temporal latch, in its simplest form, is clearly immune to upset from any single cosmic ray striking a single circuit node (a first-order effect). This is also true for TMR-based latches and for DICE-based latches. Multiple node strikes (a second-order effect), although having much lower probabilities of occurrence, will surely cause upsets when such latches are fielded in an actual space environment. The most prevalent type of multiple node strike is due to a single cosmic ray traveling through the IC at a shallow angle, nearly parallel the surface of the die, simultaneously striking two sensitive junctions. The probability of this occurring is largely geometrical with the cross section being proportional to the sensitive areas of the junctions that is normal to the incident cosmic ray and to the solid angle subtended between the these sensitive areas.

The probability of such a multiple node strike can be minimized in a circuit design by taking care in the physical layout so as to separate critical node junctions by large distances and to align such junctions so that the area of each, as viewed from the other, is minimized. For minimum sized junctions, properly aligned and separated in a carefully constructed design, the ratio of multiple node strikes to single node strikes can usually be kept on the order of  $10^{-4}$  to  $10^{-5}$ . Since, in deep-submicron layouts, first-order worst-case error rates are only on the order of  $10^{-5}$  to  $10^{-6}$  errors/bit-day, second-order worst case error rates are reduced to only  $10^{-8}$  to  $10^{-10}$  errors/bit-day. Thus, because of the increased fluency for the smaller LETs, deep submicron TMR and DICE-based implementations can be expected to display device error rates no better than their unhardened micron feature sized counterparts.

Temporal latches can, however, be easily designed to have even lower error rates. This is done (albeit with an additional layout area penalty) by implementing the temporal latch using DICE-based (or similar) latches, each of which can only be upset if two critical nodes are simultaneously struck by a heavy ion. Such a temporal latch upsets only if four critical nodes are simultaneously struck, which is easily avoided by placing the DICE-based latches such that no four critical nodes lie on any straight line.

Temporal latches designed in this fashion display at most a third-order susceptibility to cosmic ray upset. An example of a third-order event would be a cosmic ray striking two sensitive nodes in one of the latches and, at the same time, forming an SET in the combinatorial logic that arrives coincident with one of the clock edges. We have implemented several such temporal latch designs and, from the layout geometries, estimate these third-order latches to have upset rates on the order of  $10^{-15}$  errors/bit-day.

It should be apparent from these discussions that only first-order susceptible latches are capable of displaying upsets during earth-based testing. Multiple-node strikes in second-order or third-order latches cannot be produced with heavy-ion particle beams produced in tandem accelerators. The only way this might occur would be if the incident particle were to undergo a small angle Rutherford or nuclear elastic scattering. These cross sections are only on the order of a few milli-barns per steradian and can not produce significant statistics. It is still important, however, to test second and third-order latches if only to ensure that no errors have been inadvertently introduced as part of the design implementation. Such was the case with a recent heavy-ion characterization of a Xilinx part using TMR mitigation techniques [14] which displayed upsets, when none should have occurred, and indicated other error susceptibilities of the design.

### *F. Size and Speed Tradeoffs*

Clearly the temporal sampling latch occupies more area in a microcircuit than a conventional D-Flip-Flop. For typical FPGA designs, however, the impact on total device size is minimal. This is because only the D-Flip-Flops must grow -- all of the combinatorial logic in the device, including logic elements and routing, remains unchanged. If  $A_0$  denotes the original FPGA layout area,  $R$  is the ratio of D-Flip-Flop area to total FPGA area, and  $F$  is the temporal latch area penalty factor, then the new FPGA layout area  $A_1$  is given by

$$A_1 = A_0 * \{1 + (F-1)*R\}.$$

For the FPGA described in Reference [6], using a second-order immune temporal latch increases the total chip area by only 4 percent while a third-order immune temporal latch increases the area by 8 percent.

The clocking scheme of the temporal latch, shown in Figure 6, effectively increases the latch setup time and results in a lower maximum clock operating frequency. If  $F_0$  denotes the original FPGA maximum clock frequency and  $T_{bc}$  is the pulse width of each of the CLKB and CLKC phases, then the modified FPGA has a lower maximum clock frequency  $F_1$  given by

$$1/F_1 = 1/F_0 + 2*T_{bc}.$$

For an FPGA operating at a maximum frequency of 50 MHz, adding the temporal latch clocking scheme reduces the speed by 2 percent for 200 ps wide CLKB and CLKC phases.

## V. SUMMARY

We have described an SEE mitigation approach that addresses both static latch and transient induced upsets in FPGAs fabricated in deep submicron technologies and in FPGAs that incorporate EEPROM transistors within their circuitry. This new approach is based on a temporally redundant sampling latch circuit along with supporting clock generation circuitry. Not only are the usual static latch SEUs eliminated, but upsets due to SETs in the combinatorial logic, global clock, and global control signals are also eliminated. Microcircuit designs using the temporal latch are immune to these effects at any feature size. When implemented using DICE-based latches, the temporal latch can achieve immunity to multiple node cosmic ray strikes and, unlike any other SEE mitigation approach, achieve third-order susceptibility to cosmic ray induced upsets. When applied to FPGAs, the temporal latch technique has only minor impact on the physical layout size and on the speed of operation.

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