

Algorithm Level RE-computing with Shifted Operands - A Register Transfer Level Concurrent Error Detection Technique*

Kaijie Wu and Ramesh Karri

Department of Electrical Engineering

Polytechnic University

6 Metrotech Center, Brooklyn NY 11201

{kwu03@utopia,ramesh@india}.poly.edu

Abstract

Re-computing with Shifted Operands (RESO) is a logic level time redundancy based concurrent error detection (CED) technique. In RESO, logic level operations (and, nand, etc) are carried out twice - once on the basic input and once on the shifted input. Results from these two operations are compared to detect an error. Although using RESO operators in register transfer level (RTL) designs is straightforward, it entails time and area overhead. We developed an RT level CED technique called Algorithm level Re-computing with Shifted Operands (ARES0). ARES0 does not use specialized RESO operators. Rather, it exploits RT level scheduling, pipelining, operator chaining, and multi-cycling to incorporate user specified error detection latencies. ARES0 supports hardware vs. performance vs. error detection latency trade-offs. ARES0 has been validated on practical design examples using Synopsys Behavior Compiler¹.

*Supported by an NSF CAREER award CCR 996139

¹ An industry standard behavioral synthesis system