RADIATION EFFECTS ON FLASH MEMORY BASED FPGA

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FLASH SWITCH

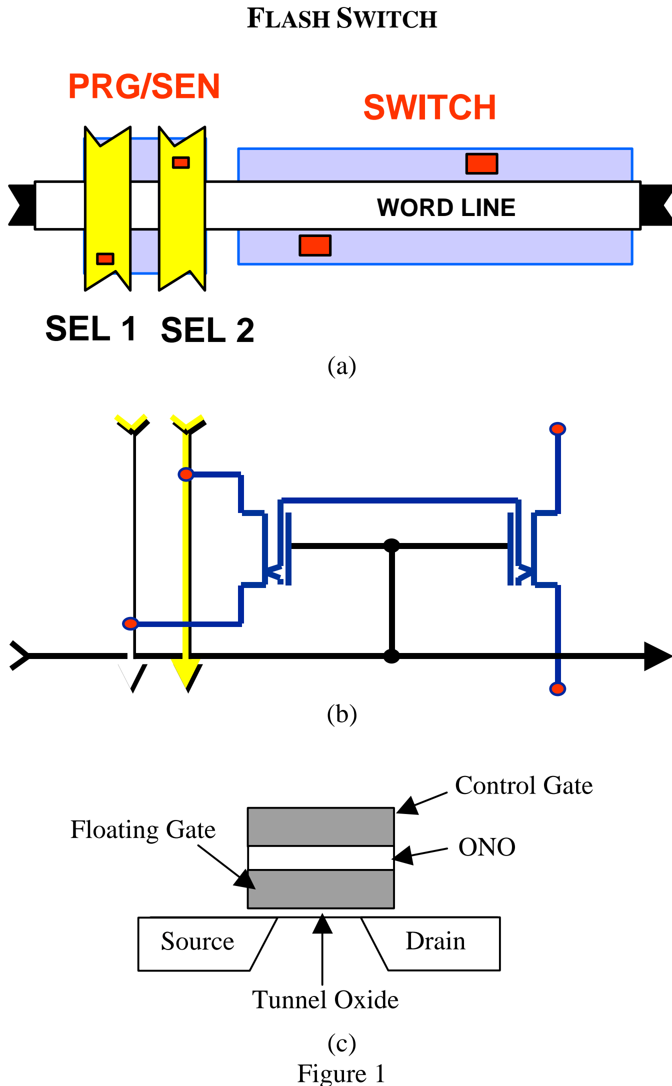

Figure 1

Any novelty in radiation effects on a FLASH memory based FPGA probably comes from the radiation effect on a configuration FLASH-memory cell. The ionizing radiation mechanisms on the logic cell are basically well studied in the passed two decades. However, as the geometry keeps shrinking, the relative importance of various radiation effects may change. Investigation of radiation effects on each technology generation is still necessary if mitigating is needed. This paper investigates the total ionization dose effects and single event effects on a state-of-the-art 0.25µm FLASH-memory based FPGA.

The switch cell consists of a program (/sense) transistor and pass transistor (Figure 1 a, b). Both transistors share a floating gate and a control gate. Figure 1c shows the cross-section of the cell structure. The switch is programmed or erased by properly biased the electrodes so that electrons will flow out of or into the floating gate by Fowler-Nordhem tunneling.

TOTAL IONIZING DOSE EFFECT

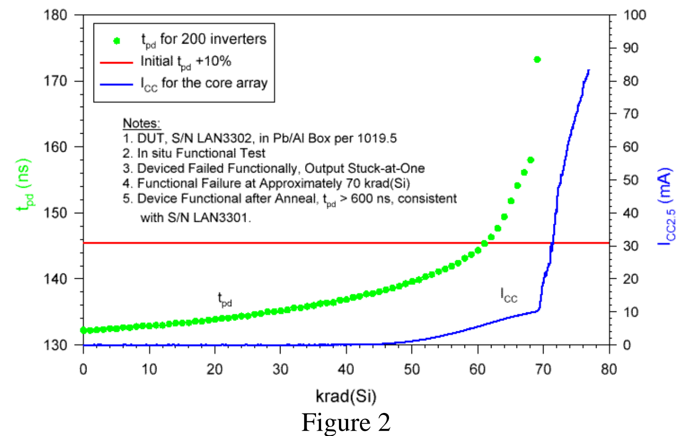

Figure 2

Figure 2 shows the total dose effect on the propagation delay and standby power supply current. The design is a long chain of buffers. The delay increase can be explained by the radiation-induced degradation of the FLASH-switch at ON-state. The leakage current increase probably comes from the transistor edge/field leakage and/or the degradation of the FLASH switch at OFF-state.

The floating gate is positively charged (relative the virgin state) to ON-state (or called programmed state) and negatively charged to OFF-state (or erased state). Once programmed, all the switches will be configured either at ON or at OFF state. Basically, the ionizing radiation causes either the ON- or OFF-state to drift closer to the virgin state.

The switch in the data path is degraded when ionizing-radiation-induced electrons/holes in the oxide migrate into or out off the float gate and neutralize the stored charges. For an ON-state switch, charge lose at the floating gate reduces the current drive and subsequently increases the propagation delay. For an OFF-state switch, charge lose at the floating gate enhances the sub-threshold leakage and increases the standby power supply current

The other possible mechanism which can reduce the charge in the floating gate is radiation induced leakage current (RILC). Irradiation can induce deep level traps in the tunneling oxide. These traps act as intermediate rest places

for the tunneling electrons and assist the neutralization of the stored charges in the floating gate.

SINGLE EVENT EFFECTS

Single event gate rupture (SEGR), single event latch-up (SEL), single event upset (SEU) and single event transient (SET) will be investigated in this paper.

The heavy ion hit on the FLASH-memory cell during programming can rupture the tunneling oxide (SEGR). The susceptibility is dependent on the LET of the heavy ion and the programming voltage. This issue is well known in the FLASH/EEPROM memory cell. The SEGR rate for FLASH-memory based FPGA would be a very small number because in-flight programming of an FPGA is very infrequent. The estimate of the LET threshold is attempted. Beam test will be followed up in the future.

SEL is studied by 3D-device simulation. The simulation results showed that if the layout is properly done, the device should be immune to heavy ion with LET up to 100 MeV-cm^2/mg. Beam test is scheduled late June and data will be available at the time of conference.

The soft error induced by SEU (single event upset) and SET (single event transient) are investigated by SPICE and 3D-device mixed mode simulation. SET in the FLASH-switch cell is one of the main focus.