

System Hardening Upset and Recovery Macro Cell Library

Submitted by

Marion Rose, Dennis Breuner, Peter Coakley

Abstract:

System hardening upset and recovery technology is being developed as a macro cell library using the legacy established under the DTRA Operate Through program. The current DTRA System Hardening Upset and Recovery (SHUR) program enhances and updates the functions of the original Operate Through Enhancement Controller (OTEC) and provides them in a hardened macro cell library for ASIC designs. The macro cells function as memory addressable “gate keeper” functions to prevent the loss of critical data and to control the recovery of a system interrupted by an upset. These performance goals are achieved by implementing the macro cells in a radiation hardened high-upset technology and also retaining the critical data in high-upset radiation hardened memory. Figure 1 illustrates the functional concept for implementing the SHUR macro cells in a protected system.

The program objective is to provide upset and recovery technology for systems designed to survive and operate through strategic nuclear levels. However, the SHUR macro cells will function equally well for any upset when detected and processed as a fault. Responses to detected faults may initiate unique recovery algorithms or sequences commensurate with the nature of the fault and the system operation and recovery design. This capability was previously developed and demonstrated under the OT program where the OTEC assumed control of the system when interrupted by a nuclear event. The SHUR program extends that technology to current system architectures and processor designs by offering flexible insertion of required upset and recovery functions at the point where they are most effective.

Performance of the SHUR macro cells is being derived from DTRA, the SPOs, and a panel of contractors based on their individual system requirements. Based on proposed system applications for SHUR technology functions, requires that the fabrication process has a dose rate upset threshold greater than $1E11$ rad(Si)/s. To achieve this high dose rate upset, the macro cell library is being designed using the Honeywell HX2000 gate array, which also enables insertion of the SHUR cells into other ASIC designs fabricated in this process. Additionally, cell designs are being reviewed and considered for migration into the Honeywell HX3000 family of gate arrays. Table 1 gives a list of the current SHUR macro cells and their status.

Implementation of the SHUR macro cells will be demonstrated with an ASIC test chip incorporating all the functions and verifying their capability to protect critical data and rapidly recover a system. Proof-of-design (PODs) ASIC demonstration devices will be characterized for radiation performance and also available for contractor evaluation. The SHUR macro cell library will be supported with performance specifications and guidelines instructing users in their ASIC application and implementation.

Further demonstration of SHUR function applications is being performed on the DTRA imager/Star Tracker to protect critical data from upset and reduce the recovery time. Selected SHUR functions are being incorporated in imaging processor ASIC and will be demonstrated in sensor radiation and hardware-in-the-loop (HWIL) tests. It is also planned to demonstrate the SHUR functions in a GPS receiver to reduce reacquisition time following an upset by storing and protecting current satellite acquisition data.

The technology developed under the SHUR program:

- Ensures command and control signal integrity
- Protects critical data
- Enables rapid recovery from upset, minimizing potential outage
- Gives flexibility to design and battle space trades
- Is a COTS enabler
- Offers upset recovery assurance

Marion Rose
Jaycor
(858) 623-3732
mrose@jaycor.com

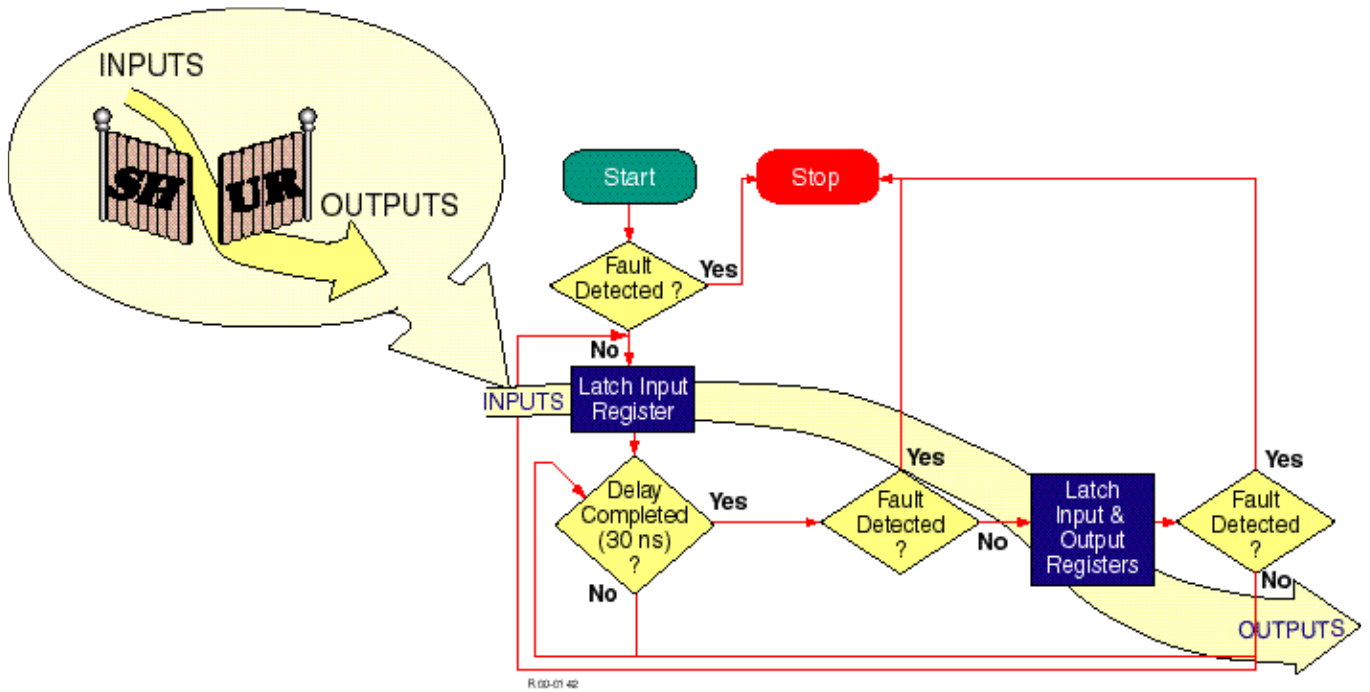


Figure 1. SHUR Macro Cells Provide Gate Keeper Protection for Command and Control Functions

Table 1. SHUR Function Status

<u>SHUR Function</u>	<u>VHDL Design</u>	<u>Testbench</u>	<u>HX2000r</u>	<u>Post-synthesis</u>
Parallel Interface	Complete	Complete	Complete	TBD
False Write Protection	Complete	Complete	Complete	TBD
Last Address Retention	Complete	Complete	Complete	TBD
Internal SRAM	Complete	TBD	TBD	TBD
Discrete Inputs	Complete	Complete	Complete	TBD
Discrete Outputs	Complete	Complete	Complete	TBD
System Clock Generation	Complete	TBD	TBD	TBD
Phase-Locked Loop	TBD	TBD	TBD	TBD
Clock Distribution	Complete	TBD	TBD	TBD
Fault Processing	TBD	TBD	TBD	TBD
Warm Start Flag	Complete	TBD	TBD	TBD
Event Counter	Complete	TBD	TBD	TBD
Off-Line Timer	Complete	TBD	TBD	TBD
Startup Timer	Complete	TBD	TBD	TBD
Command/Control I/O	Complete	TBD	TBD	TBD
Strobe Generator	Complete	Complete	TBD	TBD
Time-of-day Clock	TBD	TBD	TBD	TBD