

Ferroelectric Memory Technology for Spaceborne Applications

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Abstract

Nonvolatile memory technologies have been used in spaceborne electronic systems from the earliest computer systems. The ideal properties for such a memory, along with non-volatility are high-speed read and write cycles, radiation-hardness, and high reliability with an unlimited number of read and write cycles. The basic properties of the ferroelectric memory storage element will be discussed along with read sense and write mechanisms. This will lead to an understanding of the radiation properties of systems built with FRAM technology and an understanding of potential radiation-hardened implementations, including those at commercial foundries. Current radiation data and analysis will be presented.

I. INTRODUCTION

This summary will provide an understanding of the different materials and basic processes used for ferroelectric storage elements. The physics covering their operation and properties will be discussed in the full paper.

II. FERROELECTRIC MEMORIES

The ferroelectric RAM (FRAM) provides non-volatile storage. Architecturally, it fits in a niche between DRAM, SRAM, and EEPROM. These architectural features each contribute to the SEU effects on this class of device.

The interface to the FRAM looks similar to a synchronous SRAM. This provides a short write cycle and eliminates the long write times associated with EEPROM technology and the need for polling. Also eliminated is the high voltage circuitry and the increased chance of rupture during the write cycle, which plagues EEPROMs. The synchronous interface, however, makes the latched address, for example, vulnerable to SEUs for a non-hardened device.

Like the EEPROM, the device has a limited number of write cycles; a difference is that the device will still be functional after the limit is exceeded but it will lose non-volatility. The

FRAM is capable of a larger number of write operations, over 10^8 , while EEPROM technology supports a significantly lower number. However, like a DRAM the read is destructive and must be restored with an internally generated write cycle. When the read/write cycle limited is exceeded, there is an increase, according to the commercial specification, of the soft error rate. This suggests that an increase in the SEU rate may also be expected. The number of accesses for a device of this class must be managed as the device can not be used like a battery-backed SRAM. Fortunately, for FPGA configuration storage applications, 10^8 cycles is far more than would be needed. For microprocessor boot code storage applications, this is more of a concern, as the microprocessor can not run long out of the FRAM. The read cycle, similar to that of the DRAM, uses pre-charged bit lines and sense amplifiers which latch, followed by a restore operation. The number of read operations is limited, which differs from EEPROM technology.

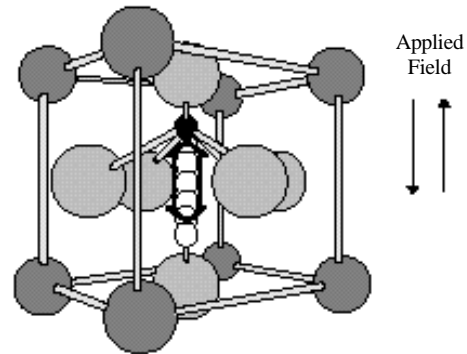


Figure 1. FRAM memory cell stores data within a crystalline structure and maintains two stable states, providing non-volatile storage. The ferroelectric film is deposited between electrode plates to form a capacitor.

Figure 1 above [RAM] shows the basic mechanism for the non-volatile storage structure. Unlike the DRAM cell, which stores charge on a capacitor or an EEPROM cell which stores charge on a gate structure, the FRAM cell stores

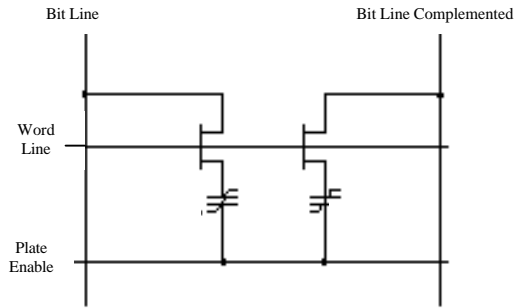


Figure 2. Two-transistor, two-capacitor (2T2C) FRAM memory cell. The differential architecture provides each bit with its own reference, eliminating capacitor variance over the die. High density memories, 1 megabit, will likely use a 1T1C cell and a global reference. Reads are destructive.

data within a crystalline structure, called a Perovskite crystal. Figure 2, below, shows a "two transistor, two-capacitor" (2T2C) topology. The two cells in this differential architecture provide a local reference. High density devices will likely use a 1T1C topology with a global reference.

Based on the brief architectural analysis above, we would expect to see SEUs independent of the hardness of the storage cell for non-hardened, COTS technology. Latches, both for digital data and in the sense amplifier, along with the pre-charged bit lines, may be susceptible. Our initial test results on both research and pre-production devices showed upsets at modest LET's; i.e., $\sim 20 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. These two sets of devices are produced at two different fabrication facilities. Other radiation effects precluded us from obtaining a large enough data set to produce a meaningful cross-section/LET curve.

Two serial FRAM devices, the FM24C16 and the FM25160, are produced at different fabrication facility (Rohm) than the FM1680. These devices did not show signs of latchup at an $\text{LET} = 74 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ when tested at $V_{\text{DD}} = 5.5\text{VDC}$. No functional testing was done on the serial devices. This initial screen was for SEL detection, only.

For the parallel FM1608 device, we observed what appeared to be latchup on the parallel FM1608 devices. For the research parts, the SEL currents ranged from 125 mA to over 800 mA, the limit programmed into the test equipment. For pre-production parts from the

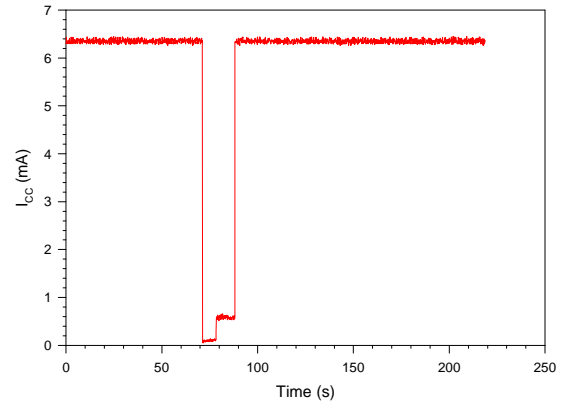


Figure 3. Strip chart of FM1608 (research fab) current during heavy ion irradiation. The device lost functionality during the test while the current decreased from its normal dynamic levels of approximately 6.3 mA to its quiescent value, near zero. The device recovered functionally and operated normally throughout the latter part of the test. This effect was seen at least three times during the limited testing of this device.

Fujitsu foundry, our three samples each latched at an LET of $18 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the lowest LET used in our test. Latchup currents observed for these devices ranged from 200 to 700 mA. Because of the low SEL_{TH} , detailed SEU measurements were not performed nor were accurate SEL cross-sections determined. Fujitsu devices with improved latchup characteristics, according to the manufacturer, are currently being shipped to our lab and will be tested in August, 1999.

SEE testing showed an additional failure mode during heavy ion irradiation of the parallel FM1608 device. In this case, the current draw of the device sharply dropped to zero, the device became non-functional, then later recovered, with the ion beam still on. A typical example is shown in Figure 3. It is seen that the current dropped from its active, dynamic level of approximately 6.3 mA to near zero, coinciding with the lost of functionality. It then increased to approximately 0.5 mA before returning to its normal, dynamic level. The device operated normally during the remainder of the test. This effect was seen at least three times during our limited testing of this set of devices. This current signature is similar to that seen in our analysis of IEEE 1149.1 JTAG structures [KAT98] and it is tempting to assume that the device entered a test mode. The manufacturer

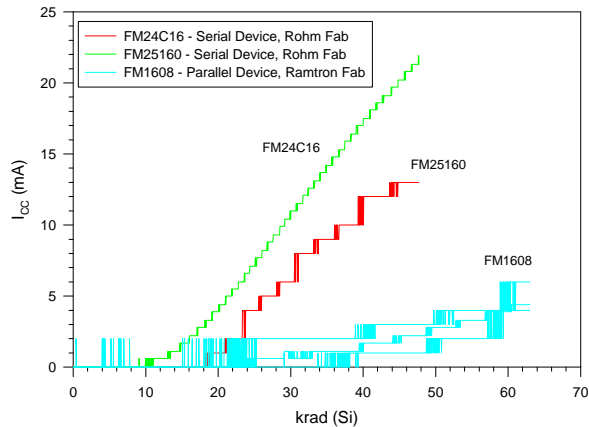


Figure 4. In situ static current measurements of two serial and one parallel FRAM device types. This initial study showed that Rohm (serial) and Ramtron research fab (parallel) devices could withstand moderate doses without significant leakage currents. Post irradiation testing of the FM1608 showed that all devices catastrophically failed. Annealing did not help. In situ functional tests or a step irradiation method are needed for determination of the functional limit. The base CMOS process is not the limiting factor for the FM1608.

indicated that this was not a plausible explanation. This temporary loss of functionality remains an open area for investigation and will be pursued in more detail when more SEL-tolerant parts are produced. From a worst-case analysis viewpoint, it is assumed that a bit gets toggled during the heavy ion test. For an actual space-flight mission, it would not get a second SEU, if that is needed, to clear the fault, resulting in system failure. Again, if SEL-tolerant devices are produced, this will be pursued, and an experiment conducted to see if the beam is required to clear the fault.

Total dose "quick-look" experiments were run on two types of serial devices and the parallel FM1608 device. In situ static current measurement data is shown in Figure 4. This exposure showed that the samples produced at Rohm and at Ramtron's research fabrication facility could withstand moderate doses without significant leakage currents. Post irradiation testing of the FM1608 showed that all devices catastrophically failed, with all locations containing the same value. Room temperature and 100°C annealing steps did not recover functionality. In situ functional tests or the more labor intensive step irradiation method is needed

for determination of the functional limit. The base CMOS process does not appear to be the limiting factor for the FM1608. It is suspected that circuits specific to the sensing/writing of the FRAM circuit element are sensitive to the total dose exposure.

III. COMMERCIAL FABRICATION

A number of commercial foundries are now developing FRAM devices. However, there is a reluctance by commercial vendors to permit the installation of a process module into their commercial line.

A purely non-invasive strategy must be employed if we are to capture the widest variety of technology. For example commercial fabs run amorphous-silicon (α -Si) anti fuse, silicon-nitride-oxide-silicon (SNOS), ferroelectric (FE), flash, and a host of other technologies. One hardening technique that requires no processing changes is a hardened by design approach. Although this design is successful at eliminating one of the leakage paths, the inter-device leakage path still remains. Further, this device is difficult to use in high-density designs because of the large amount of current drive (or effective width), it is also physically large (negating many of the benefits of modern semiconductor process technology). Another drawback is that polycrystalline-silicon contacts must be made into the center of the device (further limiting integration density) and the performance of the device is compromised at the highest levels of integration.

We have developed a novel transistor structure/process (B²JT) that is capable of radiation hardening n-channel transistors without requiring a process change to the commercial foundry. An n-channel transistor manufactured using the B²JT approach will be slightly larger than an unhardened conventional transistor, however we believe the structure/process is fully compatible with commercial foundry design rules. In certain cases we may have to violate commercial design rules but we believe that the operation of the device/IC will not be affected.