

**Radiation-Hardened/High-Reliability Programmable Logic Using Modified
Commercial-off-the-Shelf Technology**

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ABSTRACT

Logic devices for the space environment are required to perform without failure in the radiation environment. It is desirable for logic designers to have short development times, low development costs, and high density. This niche in commercial and military designs is filled by the Field Programmable Gate Array (FPGA). There are currently no completely radiation-hardened devices in existence. Devices that are used in the military and aerospace sectors are either screened commercial microcircuits or devices that have been slightly modified or "tweaked," resulting in at best a radiation-tolerant device.

The space environment and its effects on logic devices are discussed and criteria are established for radiation-hardened performance levels. The characteristics of existing devices are reviewed, both those produced at commercial and radiation-hardened foundries. Modifications to modern devices, including a new radiation-hardened flip-flop topology, are discussed and data on prototype devices is presented. By examining each radiation effect and a corresponding design technique, it is shown that a programmable logic device produced on a slightly modified commercial process is feasible.

Programmatic and technical considerations for military and aerospace electronics put specific and unique requirements on FPGA design. Along with considerations for radiation, I/O module design is critical to a microcircuit being ideally suited for these applications. These requirements and detailed engineering will be the subject of this paper. A few of the topics will be discussed below. The full paper will be complete.

I. I/O MODULE

The inherent flexibility of FPGAs is one factor that permits rapid design cycles. Indeed, for SRAM-based FPGAs, the device can be programmed in a manner similar to an embedded computer system. Antifuse-based devices require the replacement of a microcircuit. Flash-based FPGAs fall in between. However, the I/O characteristics of current FPGAs are based on commercial requirements. In this environment, multiple printed circuit board (PCB) design iterations and pre-production runs are common. With high I/O counts and output drivers with high transition times and current drive levels, PCB design is challenging. Modeling tools are expensive, are often not used, and do not guarantee success. The challenge for many low-cost space flight missions is to meet short development times and low budgets. Many programs are directed to make their first prototype units their flight unit with no engineering model.

Additionally, a characteristic of military and aerospace electronics is that multiple generations of technology are present on a single PCB. Thus, the microcircuit's input buffers and output drivers must be compatible with a wide range of I/O standards. Because of volume and mass constraints, as well as critical timing paths, adding interface devices for logic level translation is highly undesirable.

Many of the systems used in military and aerospace applications require redundancy to meet their reliability objectives. For traditional commercial CMOS devices, cold-sparing is not supported as the ESD protection diodes on the inputs and the inherent diodes in the output stage provide a

low impedance path to V_{DD} , unacceptable for these applications. While some commercial microcircuits now support hot insertion, the ability for an FPGA to support cold sparing will greatly simplify the design of many military and aerospace systems.

For critical systems, the power-on characteristics of the I/O cells have a high level of performance. This includes manned systems, weapons systems, and other electronics that control one time events such as pyrotechnic initiators. As reported last year¹, this characteristic led to the loss of a space science mission.

The design characteristics and modifications to a commercial I/O module will be discussed in the full paper.

II. STORAGE AND RADIATION

Total Dose

Modern sub-micron CMOS devices employ shallow trench isolation (STI). Previous generations used local oxidation of silicon (LOCOS). A commercial process has been modified with the results demonstrating greater than 100 krad(Si) performance for LOCOS devices and greater than 200 krad(Si) performance for 0.25 μm STI prototypes. These devices fall into the lower end of radiation-hard. Mrad(Si) level performance has not been achieved.

Single Event Latchup

All tests to date have shown that single event latchup (SEL) is not an issue for this class of devices and margins have been demonstrated.

¹ Ames, MAPLD 1999.

Single Event Upset

Single event upset (SEU) is currently the weak link in radiation performance for the space use of FPGAs. For this radiation parameter, the configuration storage architecture of the microcircuit is critical. For reprogrammable devices, depending on density, there will be from 10^5 to 10^7 storage cells. These cells can either be SRAM or Flash, for devices currently being built. Hardening that many SRAM cells is a formidable challenge. One device in development, the rebuild of the Atmel AT6010, uses a 0.8 μm SOI process to lower the probability of SEU. The A500K series of Flash-based devices, is currently under evaluation. While it is expected that the storage mechanism will have superior performance to currently available SRAM designed, the level has not yet been measured. Interestingly, the flash-based device has shown an interesting signature; as a function of total dose, tPD changes exponentially, with a performance level easily exceeding 50 krad(Si)².

Antifuse-based devices represent an affordable opportunity for SEU hardening. There are two components to this. First, the antifuse itself, while not inherently hard, has been hardened at multiple foundries. Testing has verified radiation-hard performance with large margins.³ For flip-flops, these devices have on order from 103 to 104 cells. With only a moderate number of locations to harden, relatively bulky redundancy techniques in deep sub-micron processes are feasible. The full paper will describe the design and performance measurements (both speed and SEU) of a new hardened latch, the K-cell.

² Wang, MAPLD 2000.

³ Wang, MAPLD 1999.