

# A Proven Method for High Reliability FPGA designs

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Field Programmable Gate Arrays have become a standard element for space flight instrument and spacecraft data systems. As a result of the advent of FPGA technology, it has become simple to implement in an FPGA what had once been implemented in one or more discretely designed printed circuit boards. In contrast to discretely designed printed circuit boards where most timing paths are overtly visible and fairly easy to analyze, FPGA based designs operate at much higher frequencies and can be much more difficult to analyze.

FPGA designs must now comply with aggressive cost and schedule constraints that do not allow for multiple iterations and re-designs. Following a rigorous design process enables FPGA designers to meet cost, schedule and performance for customers. By employing a regimented design process that relies on synchronous design techniques, the resulting design is one that can guarantee reliability in the operating environment over the life of the mission.

In a synchronous design, all clock inputs of storage elements are driven by the rising edges of the system clock. Storage elements range from single flip-flops to those that make up counters and state machines. Asynchronous designs utilize multiple clocks derived from combinatorial elements or outputs of clocked flip-flops to drive storage elements. Designs are also considered asynchronous when presets and clears of flip flops are used to control their outputs to perform logical functions in a design.

One of the main advantages of adhering to synchronous design techniques includes maximizing the noise immunity of the design. By utilizing only rising edges to drive all storage elements, an entire clock period is available to allow the noise generated by transitions to settle. Because these transitions account for the majority of noise generated in a design, the noise immunity is maximized.

Other advantages of a synchronous design include simplicity of design modifications and elimination of edge effects. These designs are easy to simulate, test and result in timing that is accurately and easily understood. The synchronous design concept is part of a design process that has been proven to yield high reliability FPGA designs and will be presented via a poster session at the 2000 Military and Aerospace Applications of Programmable Devices and Technologies International Conference.