Radiation-Induced Multi-bit Upsets in Xilinx SRAM-Based FPGAs

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Overview

• Background
  – Radiation-induced single-bit (SBU) and multi-bit upsets (MBU)
  – Domain crossing events

• MBU Data
  – Proton cross sections: Virtex, Virtex-II, Virtex-4
  – Heavy ion cross sections: Virtex, Virtex-II, Virtex-II Pro

• TMR Studies
  – SBU and MBU simulations
  – SEU simulation of SBU and MBUs
Background

- For SRAM-based reconfigurable devices, the state and configuration data can be subjected to radiation-induced changes
  - Most upsets are single bit upsets
  - Recently, in testing, multi-bit upsets have been observed

- Multi-bit upsets are particularly challenging for space-based applications
  - Common mitigation methods, such as triple modular redundancy, can fail in the presence of multi-bit upsets
Domain Crossing Events

- **DCE**: two or more modules from a TMR'd circuit are affected by one radiation event

- Routing networks are particularly vulnerable to DCE
  - Single-bit upsets might cause two domains to fail by shorting the routing network
  - Multi-bit upsets might be even more likely to cause two domains to fail
Research Goals

- Determine the event rate:
  - Radiation environment: multiple orbits

- Determine how frequently a single ionized particle causes multiple configuration bits to be upset
  - Feature size: multiple families of FPGAs
  - Radiation type: proton and heavy ion

- Determine how frequently DCEs occur
  - Designs: image processing, hand TMR'd (Not BYU or Xilinx tool)
  - Mitigation: multiple levels of TMR
  - SBU vs. MBU: different size events
Progress: More Questions than Answers

• Determine the event rate: no progress

• Determine how frequently a single ionized particle causes multiple configuration bits to be upset
  ✓ Feature size: multiple families of FPGAs
  ✓ Radiation type: proton and heavy ion

• Determine how frequently DCEs occur
  ✓ Early simulation results
    • Designs: non-triplicated clocks or I/O
      ✓ Isolated I/O data from results
      ? Are there clock hits in CLB results?
      ? Are multiple domains getting packed into one slice?
    • Probabilistic Model: given what we know about MBUs and our simulation results can we predict MBU DCEs?
Test Methodology

• Cross-Sections:
  – Sample configuration upsets for all architectures
  – Perform upset clustering and resource classification to identify likely MBU targets and events
  – Determine 1-bit and multi-bit cross-sections

• TMR Studies:
  – For identified functions, simulate SBU and MBU events on TMR design suite
  – Predict effect of SBUs and MBUs on TMR based on frequency of SBUs, MBUs and DCEs
Proton Analysis Highlights

- Monoenergetic testing at 63.3 MeV

- MBU Events:
  - Virtex: 0.04% of all events
  - Virtex-II: 1.08% of all events
  - Virtex-II Pro: 1.32% of all events
  - Virtex-4: 3.06% of all events

- MBU Orientation:
  - Virtex: row adjacent
  - Virtex-II, Virtex-II Pro, Virtex-4: column adjacent
  - No major column adjacencies

- Affected resources:
  - MBUs: CLBs
# Proton Bit-Cross-Sections

<table>
<thead>
<tr>
<th>Device</th>
<th>1-Bit Bit-Cross-Section (cm²/bit)</th>
<th>MBU Bit-Cross-Section (cm²/bit)</th>
<th>SEFI Cross-Section (cm²/bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCV1000</td>
<td>6.29x10⁻¹⁴</td>
<td>2.77x10⁻¹⁷</td>
<td>~4.19x10⁻¹⁹ (config SEFI)</td>
</tr>
<tr>
<td>XC2V250</td>
<td>3.06x10⁻¹⁴</td>
<td>3.34x10⁻¹⁶</td>
<td>8.21x10⁻¹⁹</td>
</tr>
<tr>
<td>XC2V1000</td>
<td>2.30x10⁻¹⁴</td>
<td>2.50x10⁻¹⁶</td>
<td>8.21x10⁻¹⁹</td>
</tr>
<tr>
<td>XC2VP40</td>
<td>3.68x10⁻¹⁴</td>
<td>4.94x10⁻¹⁶</td>
<td>Unknown</td>
</tr>
<tr>
<td>XC4VLX25</td>
<td>1.22x10⁻¹⁴</td>
<td>3.85x10⁻¹⁶</td>
<td>Unknown</td>
</tr>
</tbody>
</table>
Heavy Ion Highlights

- At highest tested linear energy transfer:
  - Virtex: saturated at 7.5% MBUs out of all events
  - Virtex-II: increasing at 35% MBUs out of all events
  - Virtex-II Pro: increasing at 34% MBUs out of all events

- MBU Orientation:
  - All devices invert from proton results
  - Very rarely does it affect to adjacent columns of resources (i.e., two adjacent CLB columns, adjacent CLB and BRAM columns, etc.)

- Affected resources:
  - SBU: CLBs, BRAM
  - MBU: CLBs, IOBs, BRAMi
Percent MBU Events Out of All Events Induced by Heavy Ion Radiation
Heavy Ion Radiation Bit Cross-Sections
TMR Test Methodology

- Three TMR designs: edge detection, max filter, min filter
- Each design has 2-3 implementations that vary module granularity
- LANL/BYU SEU simulation extended to simulate column MBUs:
  - Observe, characterize, and determine the DCE rate
  - Test both 1-bit and 2-bit column events
- August Crocker test to observe domain crossing events “in the wild”
  - Data unanalyzed
TMR Hypotheses: Bitwise Voting

- No way to recover from concurrent errors in two 1-bit modules feeding the same voter
  - When two modules change values, then the correct value in the third module looks like the incorrect result to the voter

- If two modules feeding separate voters are affected, TMR should still work
TMR Hypotheses: Domain Crossing SBUs

- Most proton-induced upsets are SBUs
  - Even rare SBUs DCEs could be more common than MBU DCEs
  - Routing network possibly vulnerable to domain crossing SBUs
  - [Bernardi-2004]: 13% of a design's used bits could cause DCEs
  - Have SBU results but not fully analyzed
Since we can't fully explain all of the SBU faults today, we're focusing on MBU faults only.
### TMR Results: MBU Sensitive Bits

#### Device: XC2V250 (Virtex-II) with 1.6 Million Bits

<table>
<thead>
<tr>
<th>Design</th>
<th>Unique MBU Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Filter (no TMR)</td>
<td>692</td>
</tr>
<tr>
<td>Max Filter (TMR Type 1)</td>
<td>122</td>
</tr>
<tr>
<td>Max Filter (TMR Type 2)</td>
<td>133</td>
</tr>
<tr>
<td>Max Filter (TMR Type 3)</td>
<td>117</td>
</tr>
<tr>
<td>Min Filter (no TMR)</td>
<td>626</td>
</tr>
<tr>
<td>Min Filter (TMR Type 1)</td>
<td>134</td>
</tr>
<tr>
<td>Min Filter (TMR Type 2)</td>
<td>135</td>
</tr>
<tr>
<td>Min Filter (TMR Type 3)</td>
<td>139</td>
</tr>
<tr>
<td>Sobel Edge (no TMR)</td>
<td>468</td>
</tr>
<tr>
<td>Sobel Edge (TMR Type 2)</td>
<td>151</td>
</tr>
<tr>
<td>Sobel Edge (TMR Type 3)</td>
<td>121</td>
</tr>
</tbody>
</table>

Even without triplicated clocks, TMR improves the cross-section 4-6 times
**TMR Results: MBU Resource Allocation**

- Design used no BRAM
- I/O failures have been removed

<table>
<thead>
<tr>
<th>Design</th>
<th>CLBs</th>
<th>BRAMi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Filter (TMR Type 1)</td>
<td>88.43%</td>
<td>7.44%</td>
</tr>
<tr>
<td>Max Filter (TMR Type 2)</td>
<td>85.59%</td>
<td>9.32%</td>
</tr>
<tr>
<td>Max Filter (TMR Type 3)</td>
<td>82.24%</td>
<td>11.21%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 1)</td>
<td>90.91%</td>
<td>6.82%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 2)</td>
<td>78.42%</td>
<td>14.39%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 3)</td>
<td>83.22%</td>
<td>7.69%</td>
</tr>
<tr>
<td>Edge Filter (TMR Type 2)</td>
<td>82.12%</td>
<td>9.27%</td>
</tr>
<tr>
<td>Edge Filter (TMR Type 3)</td>
<td>80.99%</td>
<td>2.48%</td>
</tr>
</tbody>
</table>
Given an MBU what is the probability of a DCE?

Need to determine what percentage of the event space are DCEs
# Probability of an MBU DCE in CLBs and BRAMi: Proton-Induced Radiation Events

<table>
<thead>
<tr>
<th>Design</th>
<th>BRAMi</th>
<th>CLBs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Filter (no TMR)</td>
<td>0.000010%</td>
<td>0.000964%</td>
</tr>
<tr>
<td>Max Filter (TMR Type 1)</td>
<td>0.000007%</td>
<td>0.000159%</td>
</tr>
<tr>
<td>Max Filter (TMR Type 2)</td>
<td>0.000009%</td>
<td>0.000150%</td>
</tr>
<tr>
<td>Max Filter (TMR Type 3)</td>
<td>0.000009%</td>
<td>0.000131%</td>
</tr>
<tr>
<td>Min Filter (no TMR)</td>
<td>0.000023%</td>
<td>0.000872%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 1)</td>
<td>0.000007%</td>
<td>0.000178%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 2)</td>
<td>0.000015%</td>
<td>0.000162%</td>
</tr>
<tr>
<td>Min Filter (TMR Type 3)</td>
<td>0.000009%</td>
<td>0.000176%</td>
</tr>
<tr>
<td>Edge Filter (no TMR)</td>
<td>0.000006%</td>
<td>0.000664%</td>
</tr>
<tr>
<td>Edge Filter (TMR Type 2)</td>
<td>0.000011%</td>
<td>0.000184%</td>
</tr>
<tr>
<td>Edge Filter (TMR Type 3)</td>
<td>0.000002%</td>
<td>0.000145%</td>
</tr>
</tbody>
</table>
Probability of a DCE in CLBs and BRAMi: Heavy-Ion-Induced Radiation Events
Lessons Learned

• Perfect TMR is hard to get
  – Floorplanning is very important
  – Pairs of flip flops from multiple domains could end up in one slice
  – Half latch removal could cause single points of failure
  – Would XTMR help?
    – Probably, but you'll need to triplicate I/O and control clock skew

• Reasonable TMR helps some
  – 4-6X improvement in the MBU cross-section

• The most common V-II MBU might not be bad
  – Column MBUs very low (~150 DCEs)
  – Row MBUs not tested
Conclusions and Future Work

• Space-based applications need to be aware of possible domain crossing events
  – TMR might not be perfect
  – MBUs a factor; SBUs constant background noise of faults
  – TMR-aware floorplanning and routing tools [RoRa] need to be explored for high reliability systems

• Future work:
  – Eliminate clocking issues from results
    – Designs: triplicated clocks
    – Analysis: identify routing network DCEs
  – Radiation environments
  – Reliability of reconfigurable architectures
  – Optimized scrub rates