A Dual-Use Open-Source VHDL IP library

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Extended Abstract

1 Introduction

With the availability of rad-hard high-density FPGAs such as Actel RTAX2000, it has become feasible to develop FPGA-based SOC designs also for space applications. Considering the limited volume of space hardware, the low NRE and lead-time for FPGA designs can provide a significant cost advantage over ASIC implementations. FPGA SOC solutions can favorably be used for both new designs and as a way to solve the component obsolescence problem in long-term space projects. To improve the design methodology of SOC design and to address some of the space-specific IP core requirements, Gaisler Research has developed the dual-use GRLIB IP core library, suitable for both commercial and aerospace applications. This paper will discuss the rationale and characteristics of the IP library, and present some implementation details of one of its cores: the LEON3 SPARC V8 processor.

2 GRLIB IP Library

2.1 Overview

A common, and often challenging, design tasks during SOC development is to integrate a number of third-party IP cores into a single design. This involves harmonizing bus and signal interfaces, merging of synthesis scripts and constraints, and mapping of technology specific macro cells such as memories and pads. Other issues include resolving of name clashes, and adjustment of (VHDL) library mapping. All in all, the merging of third-party IP cores is often a time-consuming and error-prone task. The rationale for the GRLIB IP library is to offset these problems by providing IP cores with a common interface and distribution format. The distribution format is designed to be extendible and vendor neutral, allowing third-party IP vendors to quickly integrate their cores into the GRLIB structure.

GRLIB is organized around VHDL libraries, where each IP vendor is assigned a unique library name. A library typically contains a number of packages, declaring the exported IP cores and their interface types. All vendor-specific files such as simulation and synthesis scripts are contained in a vendor-specific area, and automatically merged into a combined script by a global makefile. Adding and removing of libraries and packages can thus be made without modifying any global files. The initial release of GRLIB can generate scripts for the Modelsim simulator, and the Synopsys, Synplify and Xilinx XST synthesis tools. Support for other CAD tools can easily be added.

2.2 Interface and configuration

The GRLIB is designed to be ‘bus-centric’, i.e. it is assumed that most of the IP cores will be connected through a common on-chip bus. The AMBA-2.0 AHB/APB bus has been defined as the common on-chip bus, and the library includes several cores for AHB/APB arbitration and control. In addition, a novel configuration method has been added to the AHB/APB standard. The configuration method adds distributed address decoding, interrupt steering and configuration control through the use of sideband signals. This provides a plug&play capability similar to the PCI bus, while still maintaining full compatibility with the AMBA standard. When a core is attached to the on-chip bus, it is assigned an address space, interrupt number and bus index from VHDL generics. No central resource such as an address decoder or interrupt handler needs to be modified. The bus arbiter automatically generates a table (implemented as a ROM) with the vendor and device ID of all attached cores, allowing the application software (or remote debugger) to scan the on-chip bus and detect all attached cores and their configuration.

2.3 Portability

An important aspect addressed by GRLIB is portability between process technologies or macro libraries. This is done by providing an API around common technology-specific blocks such as memory and pads. A VHDL generic will specify which technology is targeted, and the appropriate memory or pad will be instantiated from the targeted technology library. Re-targeting from an FPGA to an ASIC, or between ASIC technologies, can be done by modifying a single VHDL constant, and performing a re-synthesis.

2.4 Adaptations for space use

The GRLIB IP library is intended to be used in space applications on target processes that are hardened against latch-up and total-dose radiation, but where embedded RAM blocks are sensitive to SEU. This scenario is applicable to both Actel RTAX FPGAs and most rad-tolerant ASIC processes below 0.5 µm. IP cores which use embedded RAM blocks can be configured with SEU protection through error-detection and correction. The SEU protection is implemented on a core-specific basis, in order to minimize timing penalties and draw benefit from any local redundancy. In some cases, more than one implementation is available, depending on whether an FPGA or ASIC technology is targeted. On FPGAs with spare RAM blocks, it might be better to use duplication and simple error-detection through parity, while ASIC implementations would choose a wider RAM with EDAC instead.

2.5 Available IP cores

The first release of the GRLIB IP library contains the following cores and libraries:

Common libraries: AMBA types, VHDL utilities.

IP Cores: LEON3 SPARC V8 processor, GRFPU IEEE-754 floating-point unit, 32-bit PCI target, 32-bit PCI bridge, 8/16/32-bit PROM/SRAM controller with EDAC, 32-bit SDRAM controller with EDAC, 10/100 Mbit Ethernet MAC, AHB arbiter/decoder, APB controller, multi-processor interrupt controller, 32-bit cascadable timer, generic UART, debug support unit, on-chip RAM with EDAC.

Technology wrappers: Virage SRAM, Virtex1/E/2, Actel AX/ProASIC, Atmel ATC18, Virtual Silicon RAM.

3 LEON3 SPARC V8 Processor

One of the more complex cores in the GRLIB IP library is the LEON3 SPARC V8 processor. LEON3 is a new implementation of the SPARC architecture, consisting of a 7-stage pipeline, separate multi-set caches, and a fast, purely parity-based, SEU error-correction scheme. The deep pipeline and fast error-correction scheme allows frequencies up to 400 MHz on a standard 0.13 µm process, and up to 130 MHz on a Virtex2pro FPGA. On Actel RTAX devices, 25 - 35 MHz can be reached depending on device type and processor configuration. The processor core, consisting of the pipeline, cache controllers and AHB interface, consumes approximately 20% of the resources of an RTAX2000S device. A complete SOC design comprising of a LEON3 core, PROM/SRAM controller, SDRAM controller, PCI bridge, timers, UARTs and interrupt controller, consumes less than 50% of the same device. For ASIC implementations, the same configuration will consume approximately 80 kgates, excluding embedded RAM blocks. LEON3 also includes support for multi-processor systems with up to 8 processor cores per AHB bus.

4 Availability and licensing

To facilitate early prototyping and evaluation, the major part of GRLIB is provided for free in full source code under the GNU Public License (GPL). Some cores, such the GRFPU IEEE-754 floating-point unit, are currently only provided as an FPGA netlist, while other cores such as the LEON3-FT must be licensed separately. The long-term goal for Gaisler Research is however to provide all cores under the GPL license, if the necessary funding can be raised through other activities. A traditional ‘commercial’ license for all cores is also offered, for projects where GRLIB cores will be mixed with other cores and where the GPL license cannot be applied.