



NASA Office of Logic Design

Established, February 2002



Overall Theme

A scientific study of the problems of digital engineering for space flight systems, with a view to their practical solution.

(I stole this from NACA and modified it.)



OLD Activities

- Flight Hardware Design
- Independent Reviews and Assessments
- Problem and Failure Investigations
- Design/Analysis Technique Development
- Feedback/Suggestions to Manufacturers
- Design/Analysis Seminars
- Training Classes
- Radiation Effects Testing and Mitigation
- Application Notes and Papers
- Research Projects (e.g., DDF, flight experiments, reconfigurable computing, etc.)

Rich Katz

- B.S. Stony Brook
 - Computer Science
 - Applied Math & Statistics
- M.S. Stony Brook
 - Electrical Engineering
- Jet Propulsion Lab
- Hewlett-Packard
- NASA GSFC



Interests: Design of high-reliability circuits. Use of programmable elements and devices in space-flight applications. High-performance microelectronics and signal processing applications.

Igor Kleyner

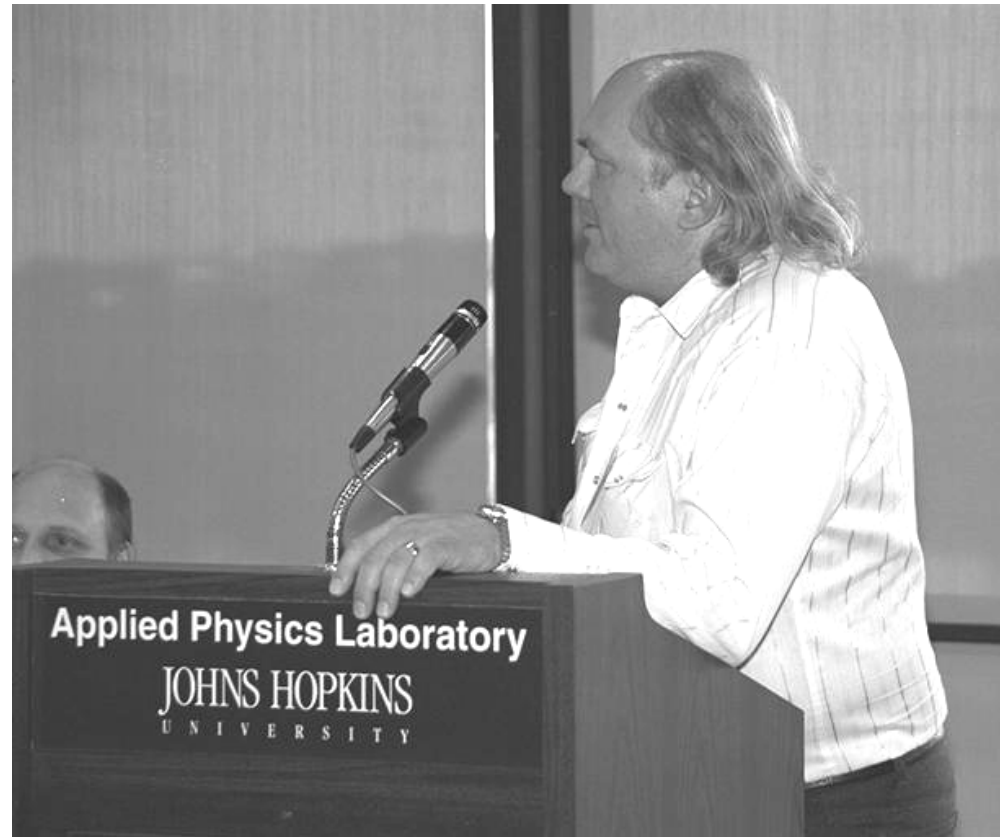
- B.S.E.E. Polytechnic University, St. Petersburg, Russia.
- M.S.E.E. Polytechnic University, St. Petersburg, Russia.
- NASA GSFC

Interests: Application of HDL's to high-reliability electronics; integration of HLLs, HDLs, IP, and test vector generation to hardware design; design and test of radiation-hardened electronics; space-flight instrument design and test.



Rod Barto

- Ph.D., U. of Texas (EE)
- M.S., U. T. El Paso (Math)
- B.S., U. T. El Paso (Math)
- College Instructor
- INTELSAT
- KLA Instruments
- Jet Propulsion Laboratory
- GE Calma
- Martin Marietta Aerospace
- Millimeter Wave Laboratory

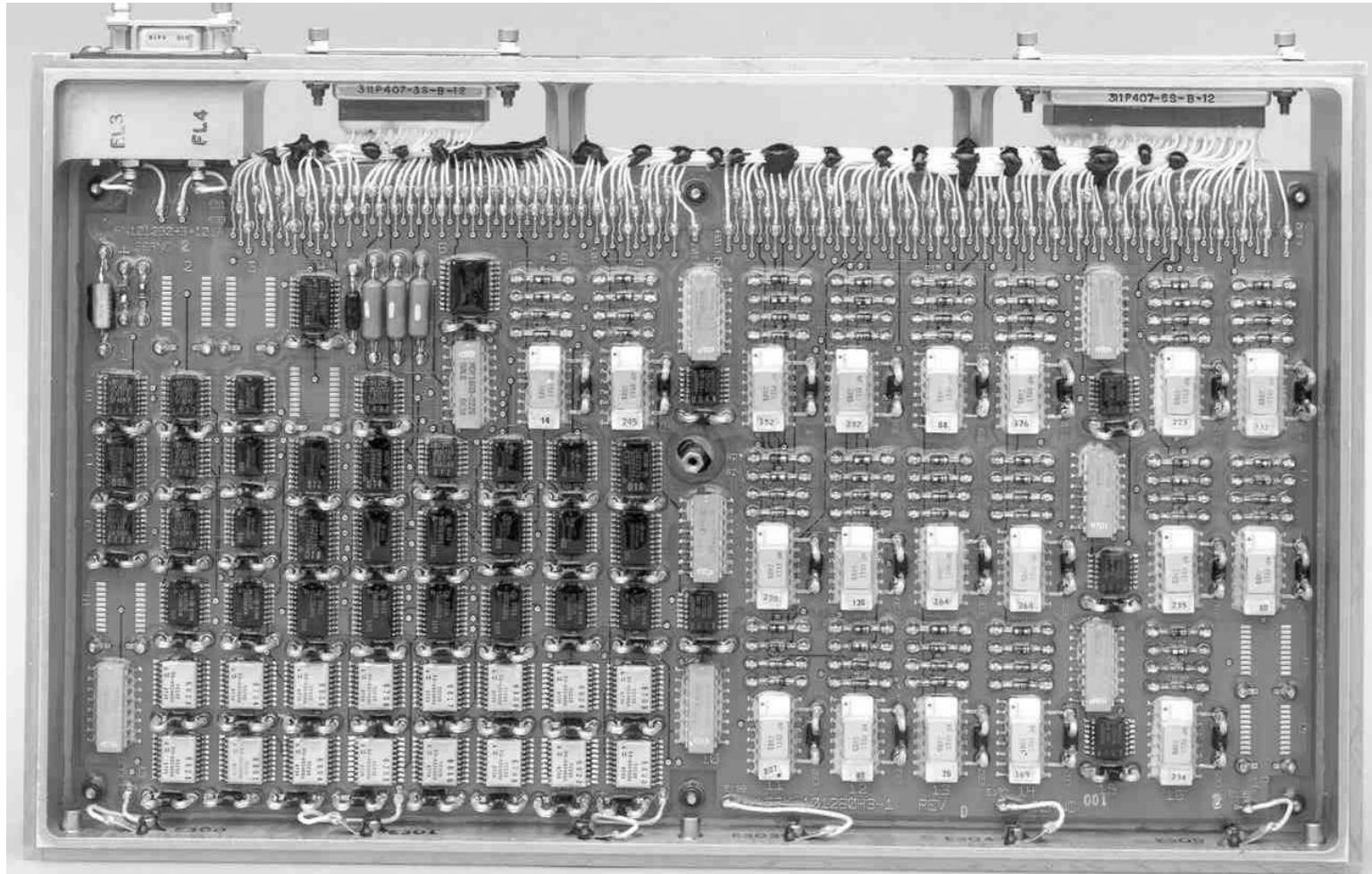


Interests: Design and analysis methodologies. Special purpose computer architectures. Fault-tolerant computers. Logic simulation accelerators.

Some Flight Projects Examples

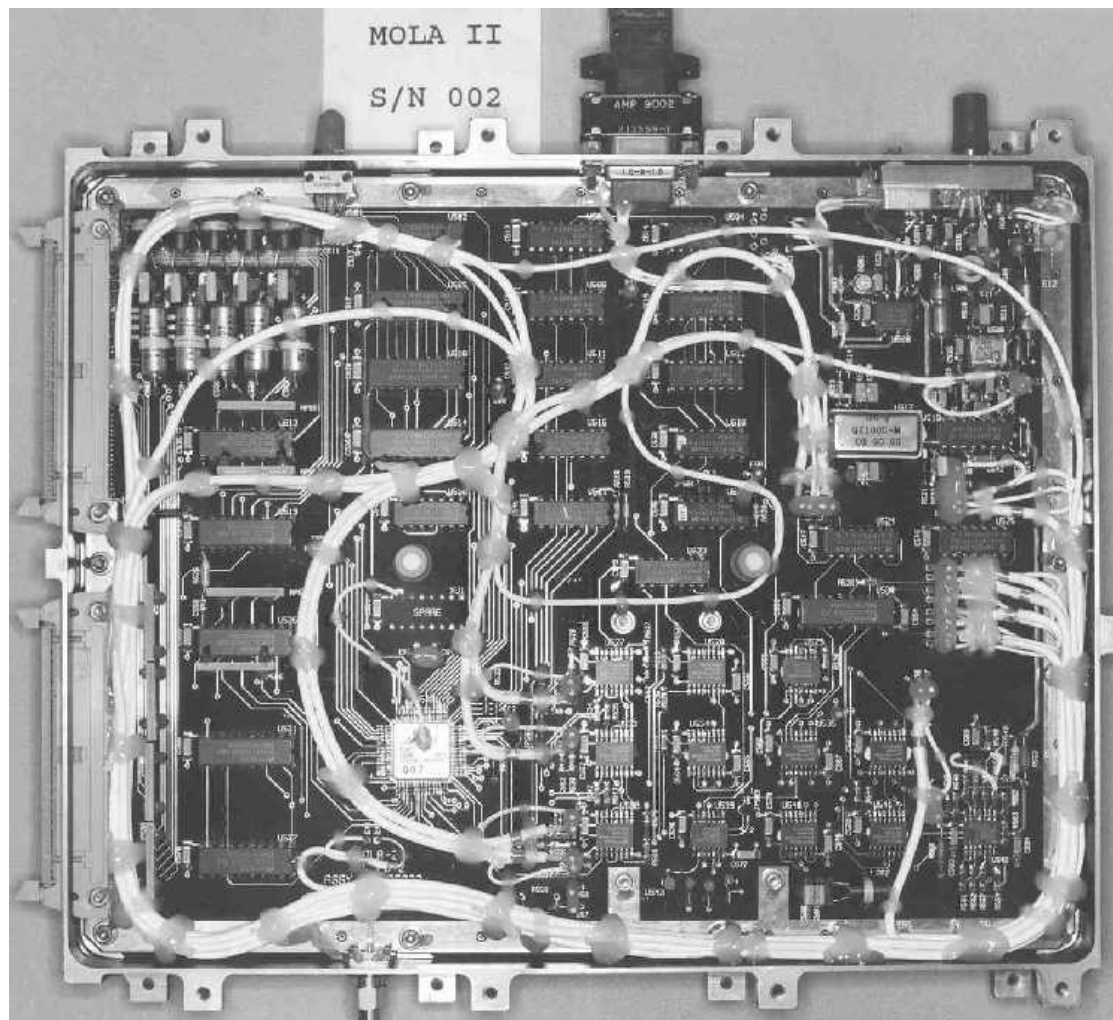
- Altimeters
 - Magellan: 1986, 442 ns
 - MOLA-II: ca. 1996, 2.5 ns
 - MESSENGER: 2002, 0.380 ns
 - Lunar Reconnaissance Orbiter (200 ps)
- Research Experiments
 - MTPB
 - STRV-1d
- Galileo
- Intelsat
- NSCAT
- SMEX Missions
- EO-1
- XDS
- ISTP (Wind, Polar)
- Cassini
- SDO

Magellan Altimeter Electronics



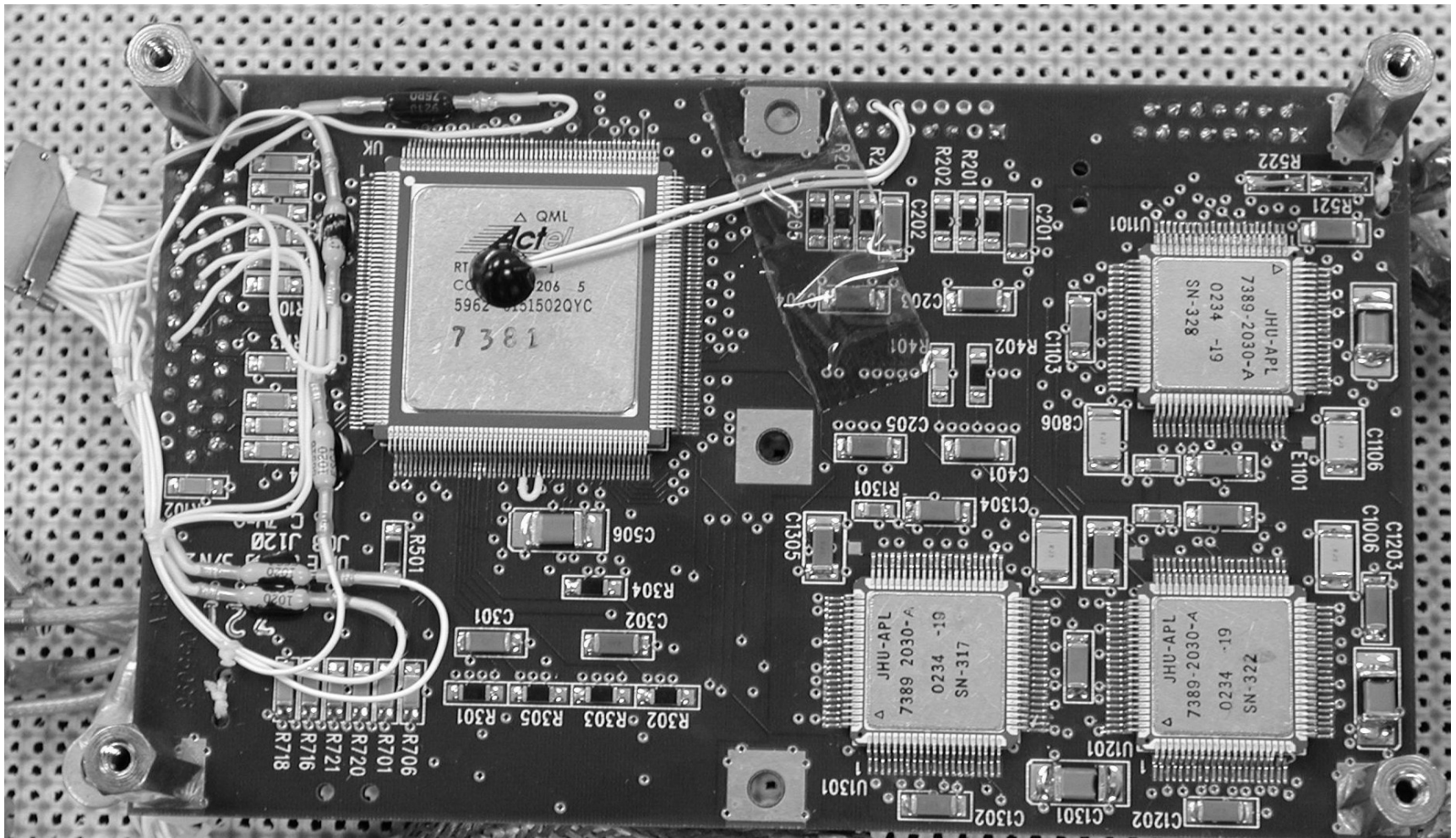
1986. 54LSxx and 54S technology; optoisolators; 4kx1 SRAM;
442 ns clock; 2,265 samples from ECL flash ADC.

MOLA-II Electronics



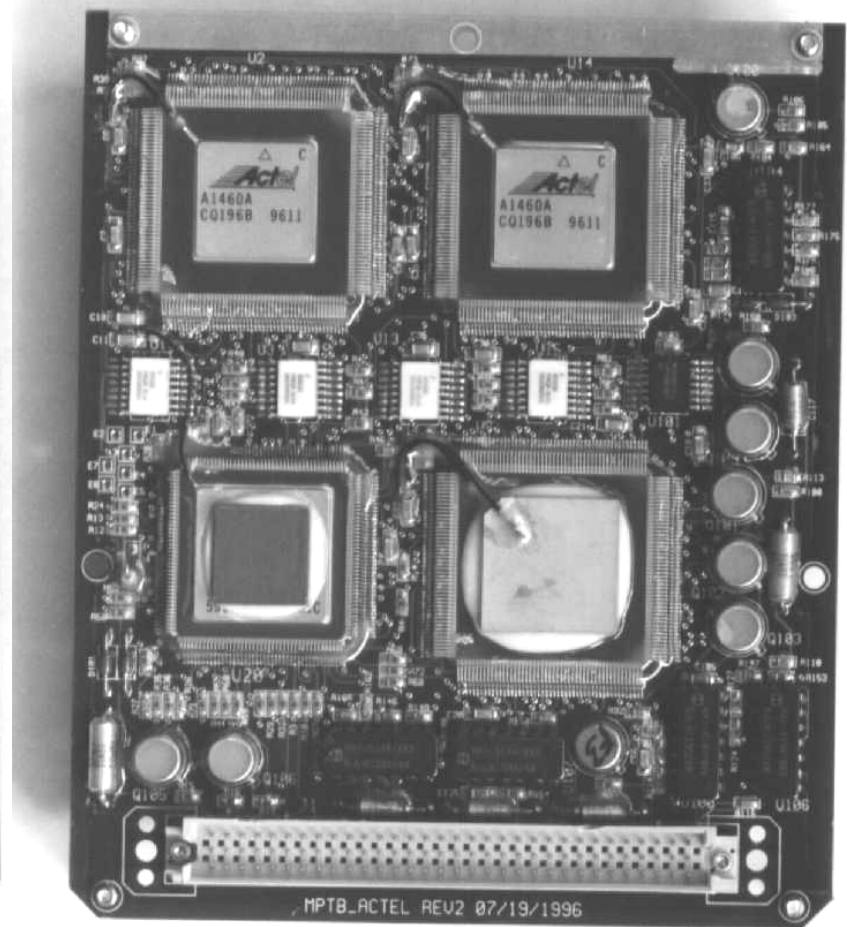
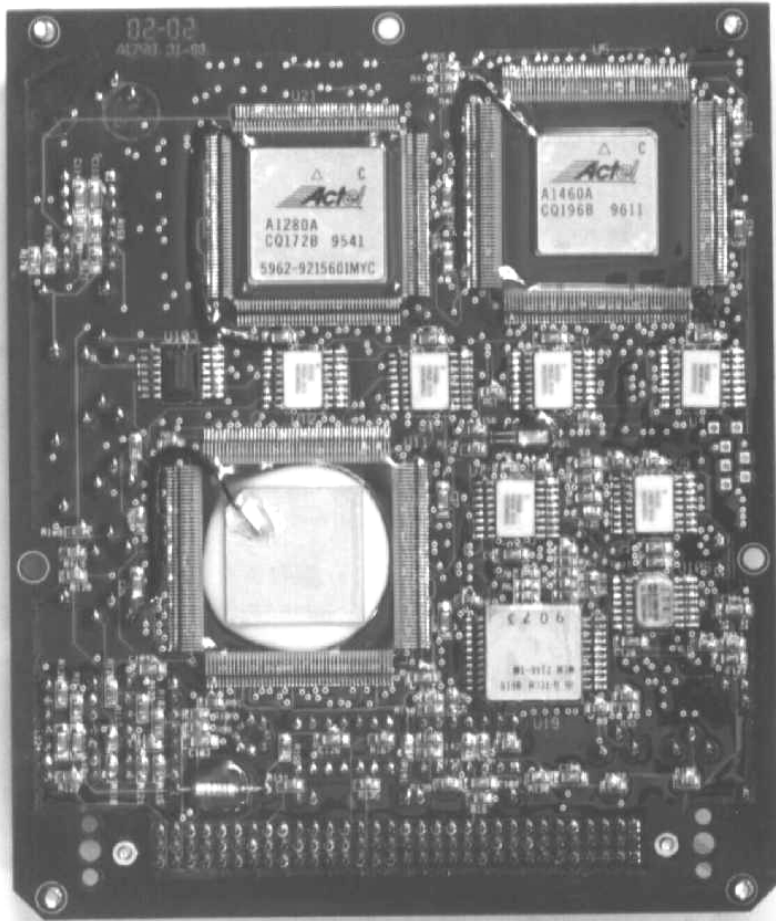
Ca. 1996. 54ACxx technology; A1020 2.0 μm FPGA; 10 ns clock w/ 2.5 ns resolution.

MESSENGER Altimeter Electronics

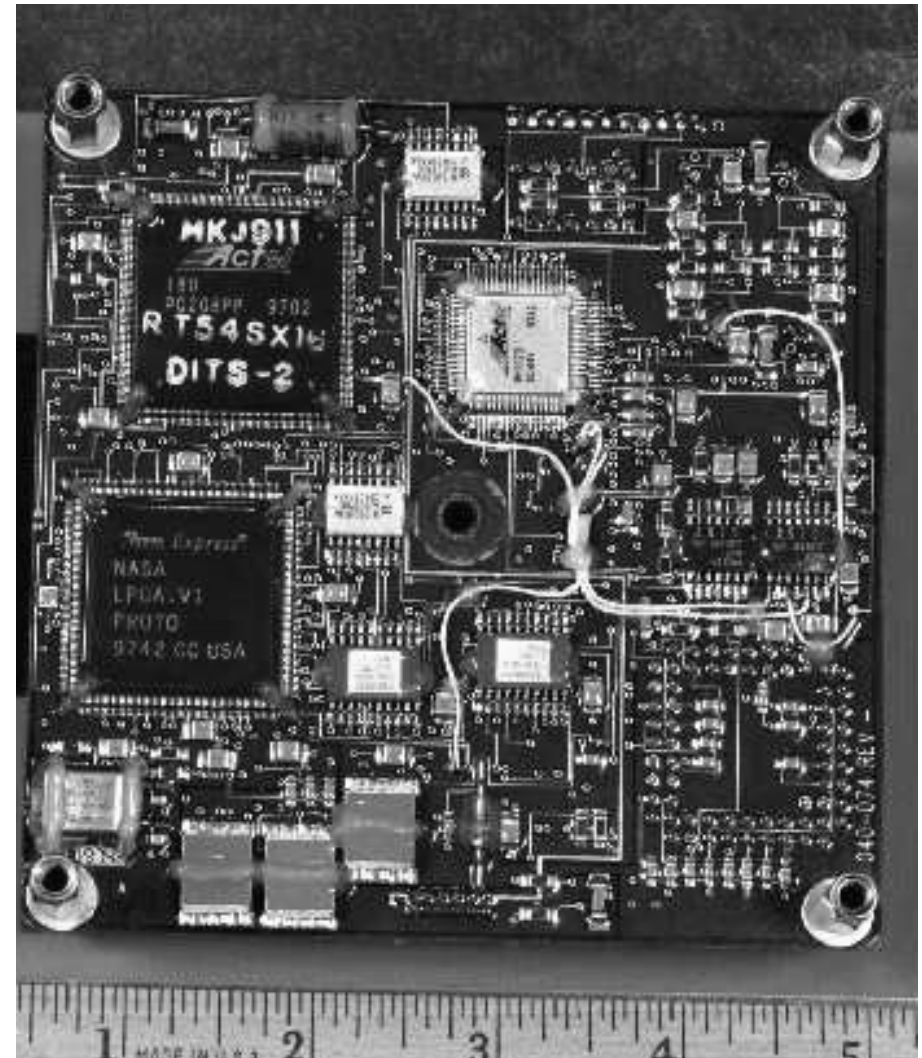
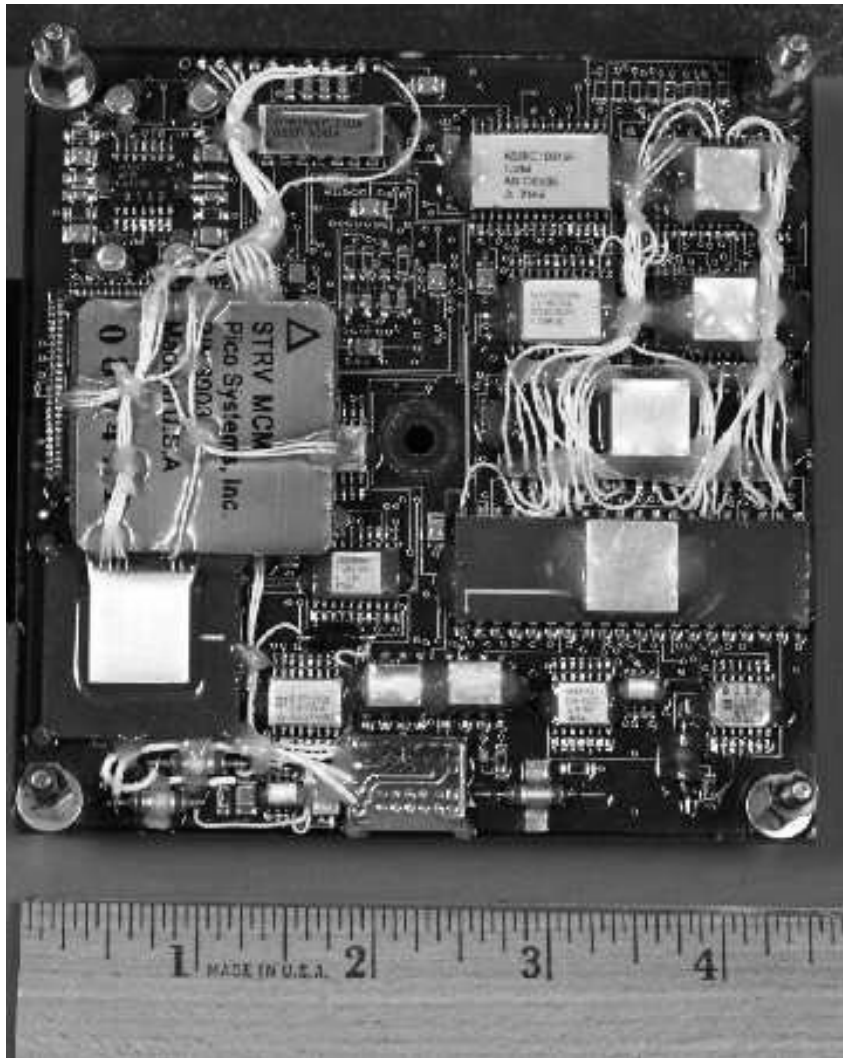


2002. RT54SXS technology. 25 MHz sequencers; embedded FIFO built from SEU-hardened registers; 380 ps resolution.

MPTB Flight Experiment



STRV-1d Flight Experiment



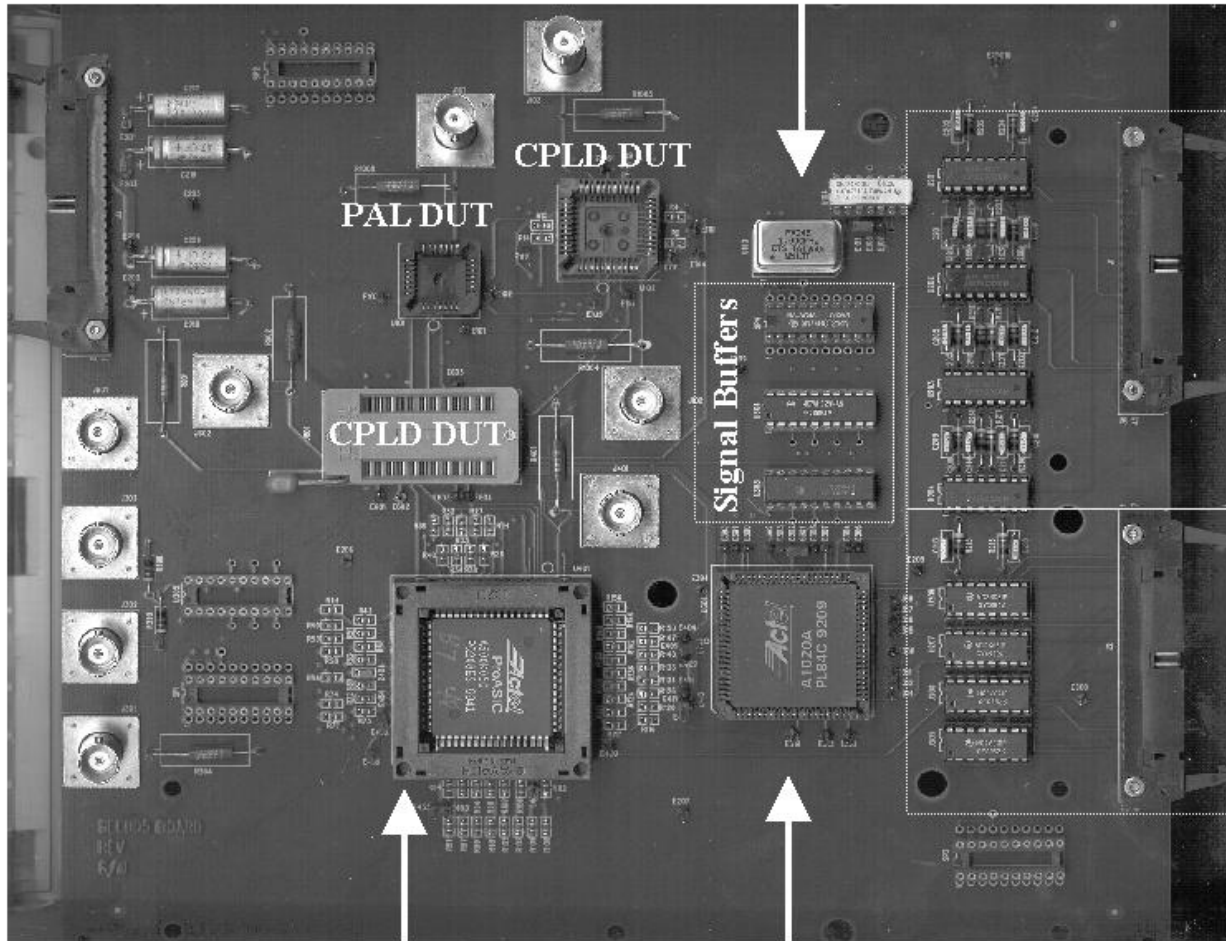
... The third in the series will be designed this year.

An SEE Radiation Test Board

TCLK Generator w/ option
to be sent from off-card

Power Interface
4 Supplies

Discrete Monitoring
Points and Buffers

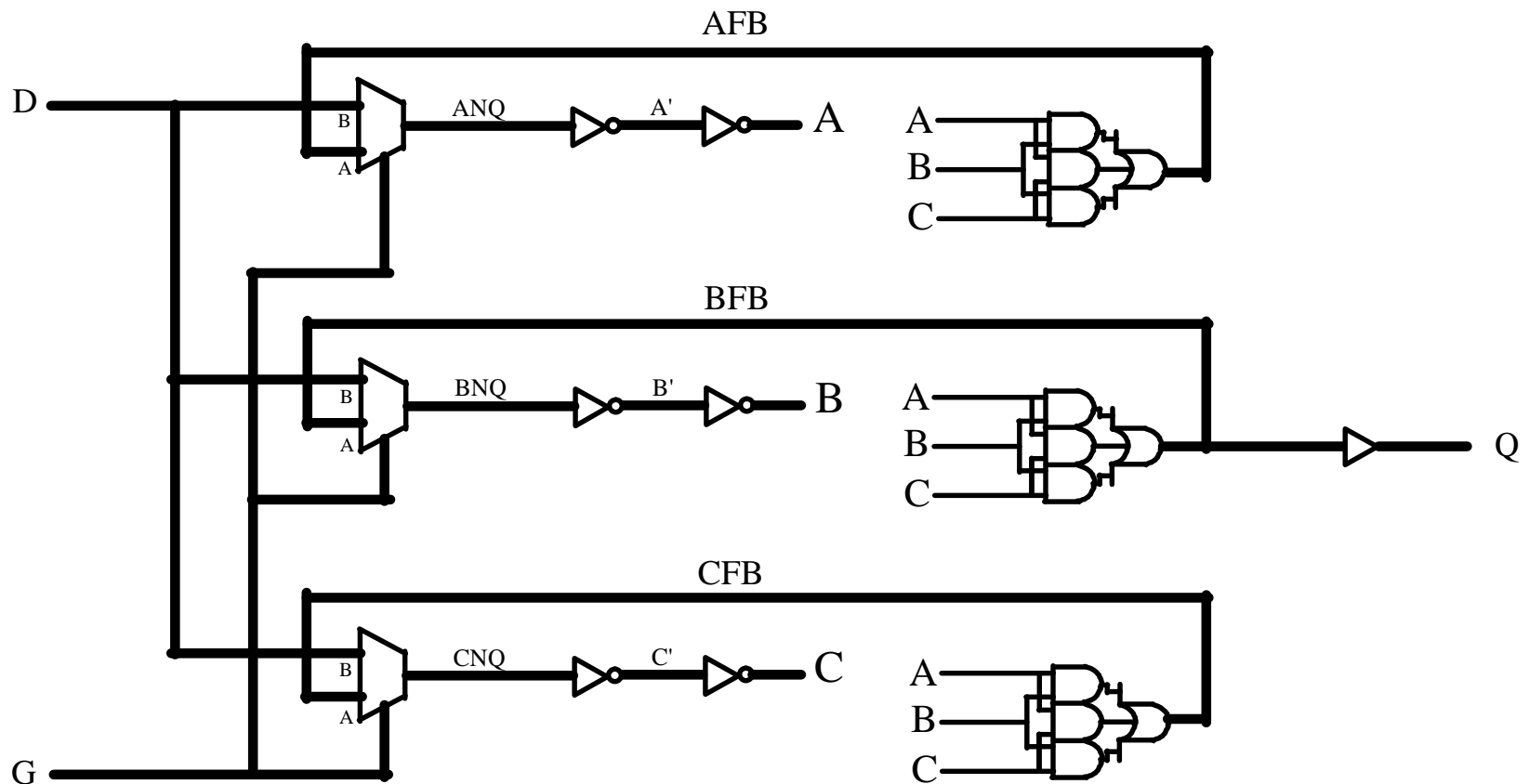


RS-422 In

RS-422 Out

Flash FPGA DUT Stimulation and Error Checking

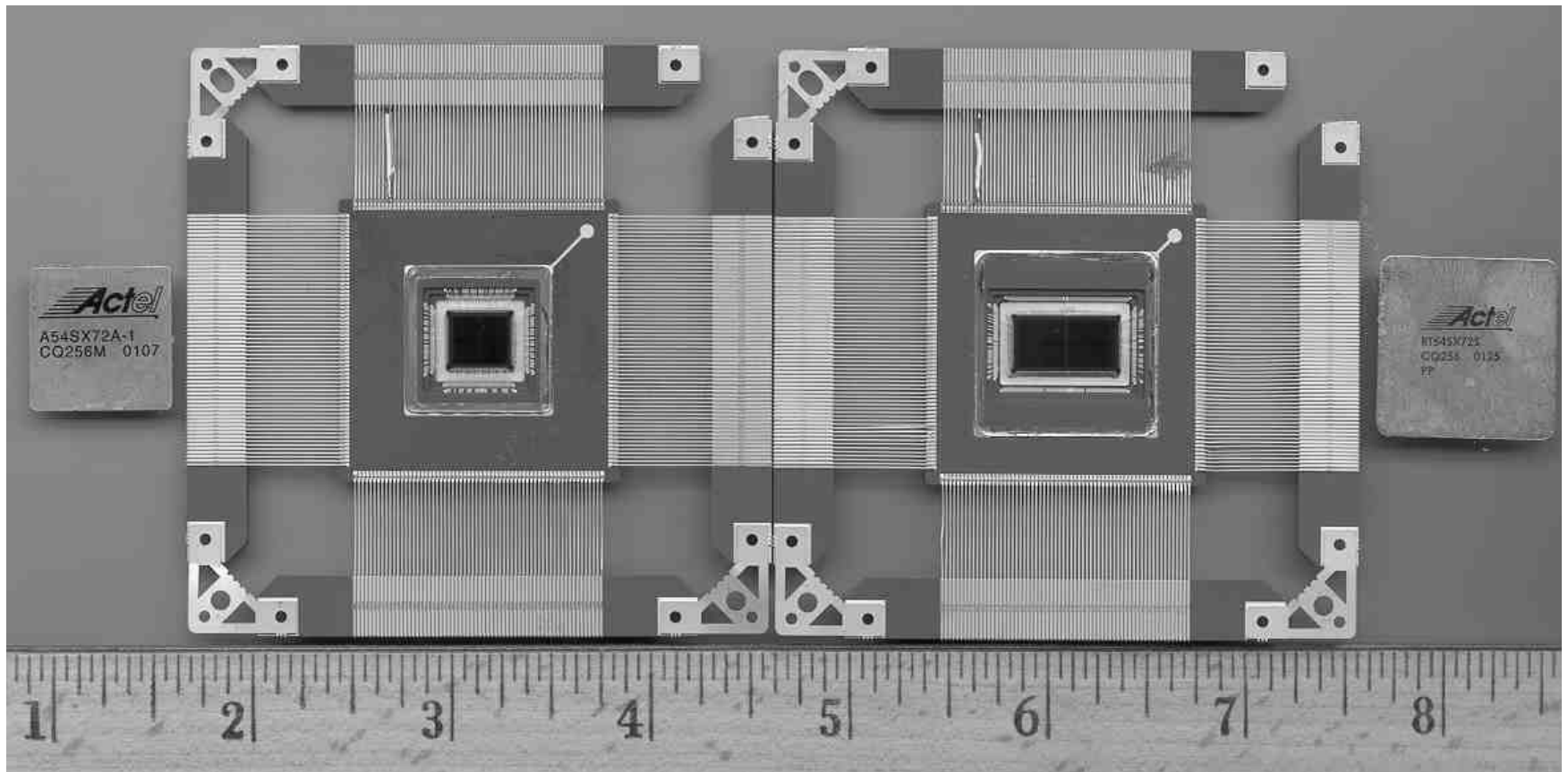
K-Latch Schematic (Simplified)



The asynchronous structure and interlocks eliminate the need for a free running clock to scrub SEUs.

Military vs. Space Grade SX72A/S

K-Latch Implemented by Industry



Some Review Activities

- Pluto: Non-Advocate Review Team
- GALEX
- GRACE
- SORCE
- HETE-2
- Space Shuttle Main Engine Vibration Monitoring System
- Second Generation Reusable Launch Vehicle
- Mars Odyssey
- AIAA Journal of Spacecraft and Rockets
- IEEE Transactions on Nuclear Science
- RADECS
- Nuclear Instruments and Methods in Physics Research
- WIRE: Lead investigator for failure mechanism.
- Calipso
- PLASTIC
- POES
- SXI
- HST/SLIC
- GLAST (just starting)
- Aqua
- HIRDLS
- GLAST
- STEREO

Communications

- WWW Site: <http://klabs.org>
- Military & Aerospace Programmable Logic Device (MAPLD) International Conference
- Journal Papers
- Application Notes, White Papers, “OLD News”
- Feedback to Vendors
 - Bugs, Alpha Testing
 - K-Latch
 - I/O Cell design, safe power-up, etc.
- OLD Brochure
- Extensive conversations with other Centers, other organizations (e.g., industry, ESA, Air Force, etc.)

Technical Conferences and Professional Society Work

- Chairman, MAPLD International Conference.
 - Co-Chairman, NASA/DoD Workshop on Evolvable Hardware.
 - Program Committee Member, Engineering of Reconfigurable Systems and Algorithms.
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- Senior Member, AIAA
 - AIAA Digital Avionics Technical Committee
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Design and Analysis Seminars

- "How Do You Review Someone Else's VHDL Design?"
 - "Programmable Logic in the Space Environment and Advanced Design Techniques"
 - "Advanced Design: Designing for Reliability"
 - "Ground Bounce"
 - "SDRAM Technology"
 - "Fundamentals of Digital Engineering: Digital Logic"
 - "Programmable Logic Devices and Architectures"
 - "Logic Design: Clocking, Timing Analysis, and State Machine Design"
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- Advanced Design: Digital Signal Processing, Programmable Device Architecture, and Military/Aerospace Applications (2003 MAPLD Int'l Conference)
 - Reconfigurable Computing: FPGA-Based, General Purpose, High Performance Systems (2003 MAPLD Int'l Conference)
 - "VHDL Do's and Don'ts" (In development)
 - "Introduction to Digital Systems Review (In development)"

Seminars (cont'd) and Training

- Seminars given at:
 - GSFC
 - MAPLD 2001, 2002
 - Marshall Space Flight Center
 - Orbital Sciences Corporation
- Seminars being planned for:
 - MAPLD 2003
 - AIAA/IEEE Digital Avionics Systems Conference
 - Johnson Space Center
 - Raytheon Corp. (in discussion)
- Training Sessions Being Planned
 - "VHDL Coding For Synthesis and Verification"
 - "Signal Integrity: Theory and Practice"

Reliable Design

Contents

- A: Introduction
- B: Special Pins
- C: Input Stages
- D: Startup Transient
- E: Hazards
- F: Asynchronous Logic
- G: Signal Quality
- H: Fail Safe Logic
- I: Reliability
- J: Power Switching
- K: Redundancy
- L: Diverse Design
- M: Configuration Control
- N: Clock Skew
- O: Processor Self Test
- P: Metastable States
- Q: Finite State Machines
- R: VHDL And Software Issues
- S: SEFI
- T: Specifications
- U: Simulators
- V: Verification
- W: Conclusion

Abstract

The concept of designing for reliability will be introduced along with a brief overview of reliability, redundancy and traditional methods of fault tolerance is presented, as applied to current logic devices. The fundamentals of advanced circuit design and analysis techniques will be the primary focus. The introduction will cover the definitions of key device parameters and how analysis is used to prove circuit correctness. Basic design techniques such as synchronous vs. asynchronous design, metastable state resolution time/arbiter design, and finite state machine structure/implementation will be reviewed. Advanced topics will be explored such as skew-tolerant circuit design, the use of triple-modular redundancy and circuit hazards, device transients and preventative circuit design, lock-up states in finite state machines generated by logic synthesizers, device transient characteristics, radiation mitigation techniques, worst-case analysis, the use of timing analyzers and simulators, and others. Case studies and lessons learned from spaceflight designs will be given as examples.