

NOTICE OF REVISION (NOR)		1. DATE (YYMMDD) 96-06-24	Form Approved OMB No. 0704-0188
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.			
<small>Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.</small>		2. PROCURING ACTIVITY NO.	3. DODAAC
		4. ORIGINATOR	5. CAGE CODE 67268
a. TYPED NAME (First, Middle Initial, Last)	b. ADDRESS (Street, City, State, Zip Code) Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	7. CAGE CODE 67268	8. DOCUMENT NO. 5962-93091
9. TITLE OF DOCUMENT MICROCIRCUIT, HYBRID, MEMORY, 512K X 8-BIT, ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY	10. REVISION LETTER	11. ECP NO.	
	a. CURRENT B	b. NEW C	N/A
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All			
13. DESCRIPTION OF REVISION			
<p>Sheet 1: Revisions ltr column; add "C". Revisions description column; add "Changes in accordance with NOR 5962-R154-96". Revisions date column; add "96-06-24". Revision level block; change from "B" to "C". Rev status of sheets; for sheets 1,3, and 4; change from "B" to "C".</p> <p>Sheet 3: Paragraph 1.3; add "Endurance-10,000 cycles minimum". Revision level block; change "B" to "C".</p> <p>Sheet 4: Add the following paragraphs 3.9, 3.10, and 3.11:</p> <p>"3.9 <u>Programming procedure</u>. The programming procedure shall be as specified by the manufacturer and shall be available upon request.</p> <p>3.10 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendors procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.</p> <p>Continued on sheet 2.</p>			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a. (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ELDT		c. TYPED NAME (First, Middle Initial, Last) Kendall A. Cottongim	
d. TITLE Chief, Electronic Components Branch	e. SIGNATURE Kendall A. Cottongim		f. DATE SIGNED (YYMMDD) 96-06-24
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ELDT	b. REVISION COMPLETED (Signature) Gary Zahn		c. DATE SIGNED (YYMMDD) 96-06-24

13. DESCRIPTION OF REVISION - CONTINUED

Document No.: 5962-93091
Revision: c
NOR No.: 5962-R154-96
Sheet: 2 of 2

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity."

Revision level block; change "B" to "C".

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN: add "2" to SMD PIN 5962-9309104HXX. Also, add the following: "2/ Case outline X is no longer available and not recommended for new design. Case outline Y can be substituted for case outline X." below note 1 under Pin table.

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Added device type 05. Added case outline Y. Redrew entire document.	96-04-22	K.A. Cottongim



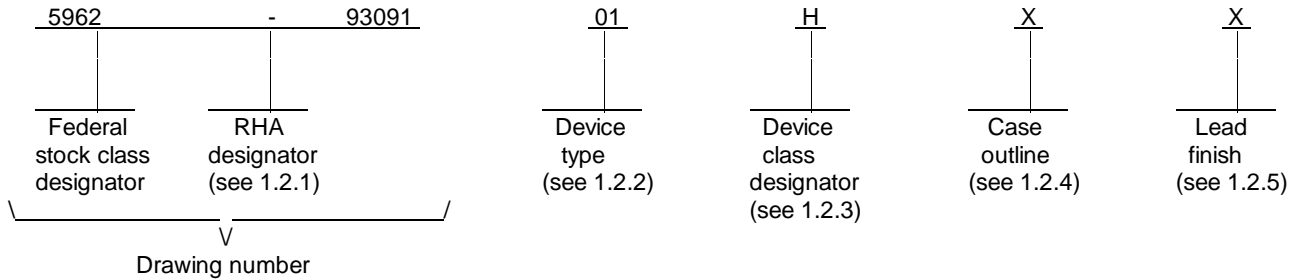
REV																				
SHEET																				
REV	B	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20	21													
REV STATUS OF SHEETS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Steve L. Duncan	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Michael Jones		
	APPROVED BY Kendall A. Cottongim		
	DRAWING APPROVAL DATE 93-01-22		
	REVISION LEVEL B		
	MICROCIRCUIT, HYBRID, MEMORY, 512K X 8-BIT, ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY		
AMSC N/A	SIZE A	CAGE CODE 67268	5962-93091
SHEET 1 OF 21			

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-H-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	WE-512K8-150CQ	EEPROM, 512K x 8-bit	150 ns
02	WE-512K8-300CQ	EEPROM, 512K x 8-bit	300 ns
03	WE-512K8-250CQ	EEPROM, 512K x 8-bit	250 ns
04	WE-512K8-200CQ	EEPROM, 512K x 8-bit	200 ns
05	WE-512K8-200CQ	EEPROM, 512K x 8-bit	200 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	32	Dual-in-line, dual cavity
Y	See figure 1	32	Dual-in-line, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 2

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.6 V dc to +6.25 V dc
Input voltage range	-0.6 V dc to +6.25 V dc
Power dissipation (P _D)	1.6 W
Storage temperature range	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+300° C
Thermal resistance, Junction to case (θ _{JC})	28° C/W
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range	+4.5 V dc to +5.5 V dc
Input low voltage range (V _{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V _{IH})	+2.2 V dc to V _{CC} + 0.3 V dc
Output voltage, High minimum (V _{OH})	+2.4 V dc
Output voltage, Low maximum (V _{OL})	+0.45 V dc
Case operating temperature range (T _C)	-55° C to +125° C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

PERFORMANCE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5, 6, 7, and 8.

3.2.5 Block diagram. The block diagram shall be as specified on figure 9.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-PRF-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DESC-EL) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DESC-EL shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55° C ≤ T _C ≤ +125° C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits Unit	
					Min	Max

DC PARAMETERS

Supply current	I _{CC}	$\overline{CS} = \overline{OE} = V_{IL}$, WE = V _{IH} , I/O 0 through I/O 7 = open, inputs = V _{CC} = 5.5 V dc, A0 through A18 change at 5 MHz	1, 2, 3	All		180	mA
Standby current	I _{SB}	$\overline{CS} = V_{CC}$, I/O 0 through I/O 7 = open, inputs = V _{CC} = 5.5 V dc, A0 through A18 change at 5 MHz	1, 2, 3	All		10	mA
Input leakage current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All		80	μA
Output leakage current	I _{LO}	V _{OUT} = V _{SS} to V _{CC} , CS = V _{IH}	1, 2, 3	All		80	μA
Input low voltage	V _{IL}		1, 2, 3	All		0.8	V
Input high voltage	V _{IH}		1, 2, 3	All	2.0		V
Output low voltage	V _{OL}	I _{OL} = 2.1 mA, V _{CC} = +4.5 V	1, 2, 3	All		0.45	V
Output high voltage	V _{OH}	I _{OH} = -400 μA, V _{CC} = +4.5 V	1, 2, 3	All	2.4		V

FUNCTIONAL TESTING

Functional tests		See 4.3.1c	7, 8A, 8B	All			
V _{CC} sense write inhibit	V _{SENS}	See 4.3.1c	7, 8A, 8B	05	3.0	4.3	V
V _{CC} Power on delay write inhibit	V _{POD}	See 4.3.1c	7, 8A, 8B	05		10	mS

DYNAMIC CHARACTERISTICS

Input capacitance	C _{IN}	V _{IN} = 0 V dc 2/	4	All		90	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V dc 2/	4	All		120	pF

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55° C ≤ T _C ≤ +125° C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits Unit		
					Min	Max	
READ CYCLE AC TIMING CHARACTERISTICS							
Read cycle time	t _{RC}	See figure 4	9, 10, 11	01 02 03 04,05	150 300 250 200		ns
Address access time	t _{ACC}	See figure 4	9, 10, 11	01 02 03 04,05		150 300 250 200	ns
Chip select access time	t _{ACS}	See figure 4	9, 10, 11	01 02 03 04,05		150 300 250 200	ns
Output hold from address change OE or CS	t _{OH}	See figure 4	9, 10, 11	All	0		ns
Output enable to output valid	t _{OE}	See figure 4	9, 10, 11	01,04,05 02 03	85	ns 125 100	

BYTE WRITE AC TIMING CHARACTERISTICS

Address setup time	t _{AS}	See figure 5	9, 10, 11	All	10		ns
Write pulse width	t _{WP}	See figure 5	9, 10, 11	01-04	150		ns
		See figure 5, t _{CS} > 50 ns		05	110		
Chip select setup time	t _{CS}	See figure 5	9, 10, 11	All	0		ns
Address hold time	t _{AH}	See figure 5 3/	9, 10, 11	All	125		ns
Data valid to end of write	t _{DV}	See figure 5	9, 10, 11	All	100		ns
Output enable setup time	t _{OES}	See figure 5	9, 10, 11	All	10		ns
Data hold time	t _{DH}	See figure 5	9, 10, 11	All	10		ns
Output enable hold time	t _{OEH}	See figure 5	9, 10, 11	All	10		ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55° C ≤ T _C ≤ +125° C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits Unit	
					Min	Max

BYTE WRITE AC TIMING CHARACTERISTICS - Continued

Chip select hold time	t _{CSH}	See figure 5	9, 10, 11	All	0 ^{4/} 25 ^{5/}		ns
Write pulse widthhigh	t _{WPH}	See figure 5	9, 10, 11	All	50		ns

PAGE MODE WRITE AC TIMING CHARACTERISTICS

Data setup time	t _{DS}	See figure 6	9, 10, 11	All	100		ns
Data hold time	t _{DH}	See figure 6	9, 10, 11	All	10		ns
Write pulse width	t _{WP}	See figure 6	9, 10, 11	All	150		ns
Byte load cycle time	t _{BLC}	See figure 6	9, 10, 11	All		150	μs
Write pulse widthhigh	t _{WPH}	See figure 6	9, 10, 11	All	50		ns
Write cycle time	t _{WC}	See figure 6	9, 10, 11	All		10	ms

DATA POLLING AC TIMING CHARACTERISTICS

Data hold time	t _{DH}	See figure 7	9, 10, 11	All	10 ^{4/} 35 ^{5/}		ns
Output enableholdtime	t _{OEH}	See figure 7	9, 10, 11	All	10 ^{4/} 35 ^{5/}		ns
Output enabletooutput delay	t _{OE}	See figure 7	9, 10, 11	All		100	ns
Write recovery time	t _{WR}	See figure 7	9, 10, 11	All	0		ns

See footnotes at end of table

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55° C ≤ T _C ≤ +125° C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CHIP ERASE CHARACTERISTICS							
Setup time 6/	t _S	See figure 8	7,8A,8B	05	5		μs
Pulse width 6/	t _W	See figure 8	7,8A,8B	05	10		ms
Chip erase voltage	V _H		7,8A,8B	05	11.4	12.6	V
Hold time 6/	t _H	See figure 8	7,8A,8B	05	5		μs

1/ Unless otherwise specified; the AC test conditions are as follows:

Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.

Input rise and fall times: 5 ns.

Input and output timing reference levels: 1.5 V.

2/ Parameters shall be tested as part of device characterization and after design and process changes.

Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

3/ A17 and A18 must remain valid through the WE or CS low pulse.

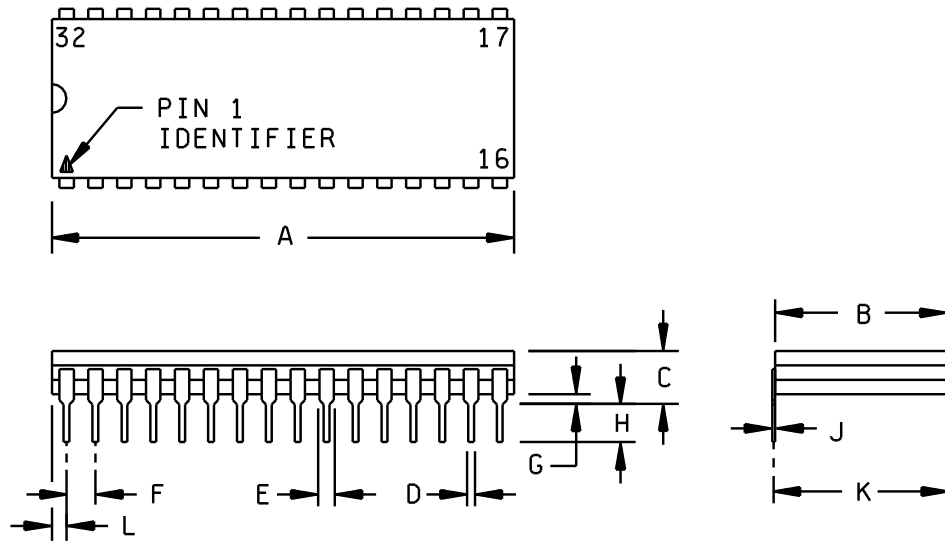
4/ WE controlled

5/ CS controlled

6/ Data FF for all addresses following sequence.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 8

Case outline X



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	1.654	1.686	42.01	42.82
B	0.580	0.600	14.73	15.24
C	0.235	0.275	5.97	6.99
D	0.016	0.020	0.41	0.51
E	0.045	0.055	1.14	1.40
F	0.100 TYP.		2.54 TYP.	
G	0.015	0.060	0.38	1.52
H	0.125 MIN.		3.18 MIN.	
J	0.008	0.012	0.20	0.30
K	0.590	0.610	14.99	15.49
L	0.085 TYP.		2.16 TYP.	

FIGURE 1. Case outline.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

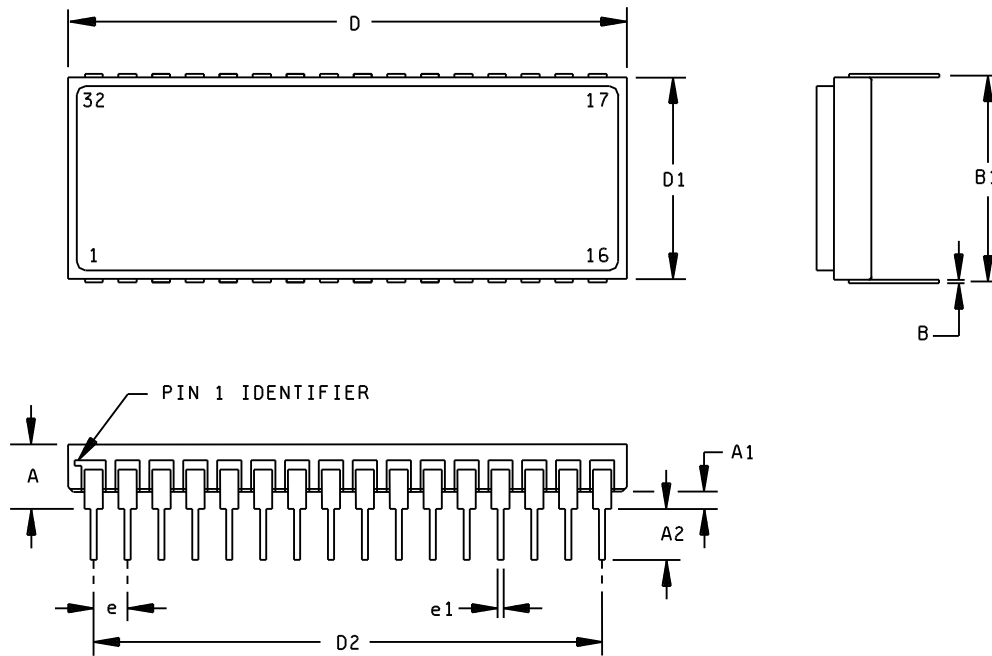
SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
9

Case outline Y



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
D	1.654	1.686	42.01	42.82
D1	0.580	0.600	14.73	15.24
A	0.161	0.181	4.10	4.60
e1	0.016	0.020	0.41	0.51
D2	1.492	1.508	38.02	38.30
e	0.100 TYP.		2.54 TYP.	
A1	0.027	0.047	0.69	1.14
A2	0.125 MIN.		3.18 MIN.	
B	0.009	0.012	0.23	0.30
B1	0.590	0.610	14.99	15.49

NOTE: The U.S. government preferred system of measurement is the metric SI. These case outlines were designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 10

Device types	01-05
Case outline	X and Y
Terminal number	Terminal connection
1	A18
2	A16
3	A15
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0
13	I/O 0
14	I/O 1
15	I/O 2
16	V _{SS}
17	I/O 3
18	I/O 4
19	I/O 5
20	I/O 6
21	I/O 7
22	CS
23	A10
24	OE
25	A11
26	A9
27	A8
28	A13
29	A14
30	A17
31	WE
32	V _{CC}

FIGURE 2. Terminal connections.

\bar{CS}	\bar{OE}	\bar{WE}	A0-A18	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	H	L	Stable	Write	Data In	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write inhibit	High Z/Data out	Active
X	L	X	X	Write inhibit	High Z/Data out	Active

NOTES:

1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either High or Low)
4. High Z = High Impedance state

FIGURE 3. Truth table.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 11

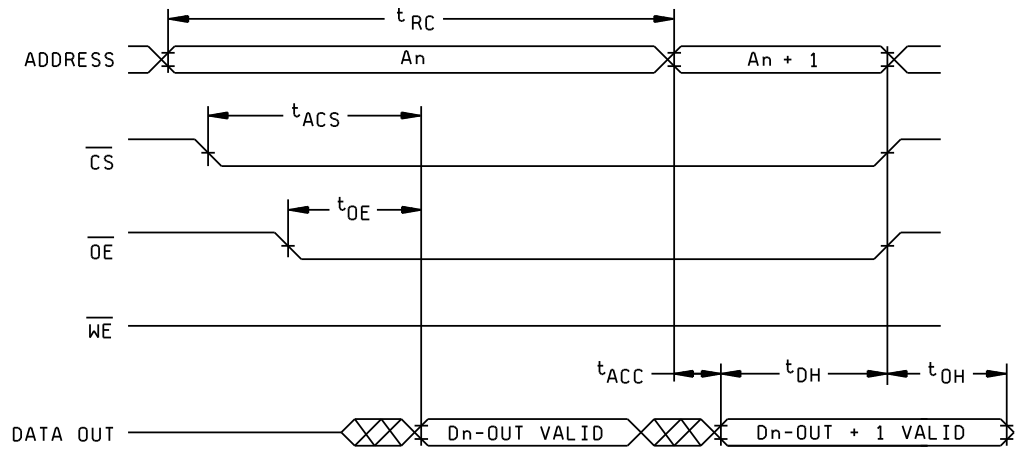


FIGURE 4. Read cycle timing diagram.

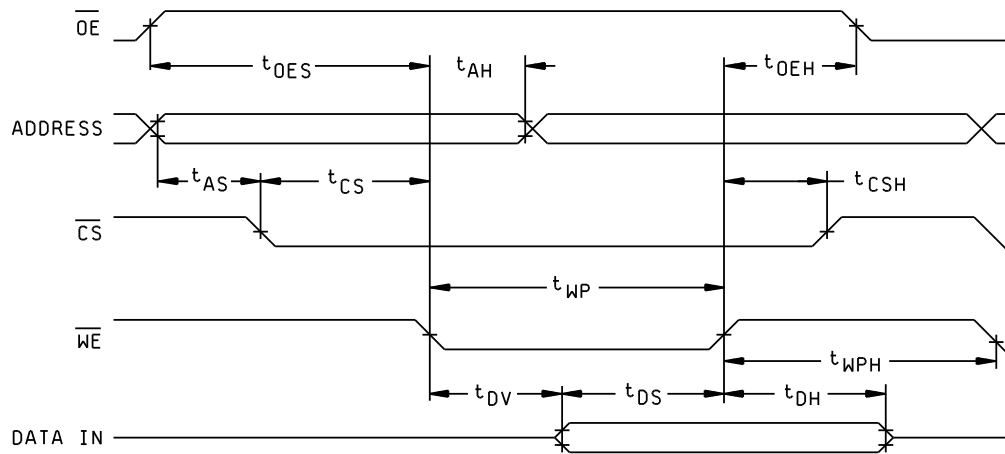
STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
12



\overline{WE} controlled

FIGURE 5. Write cycle timing diagram.

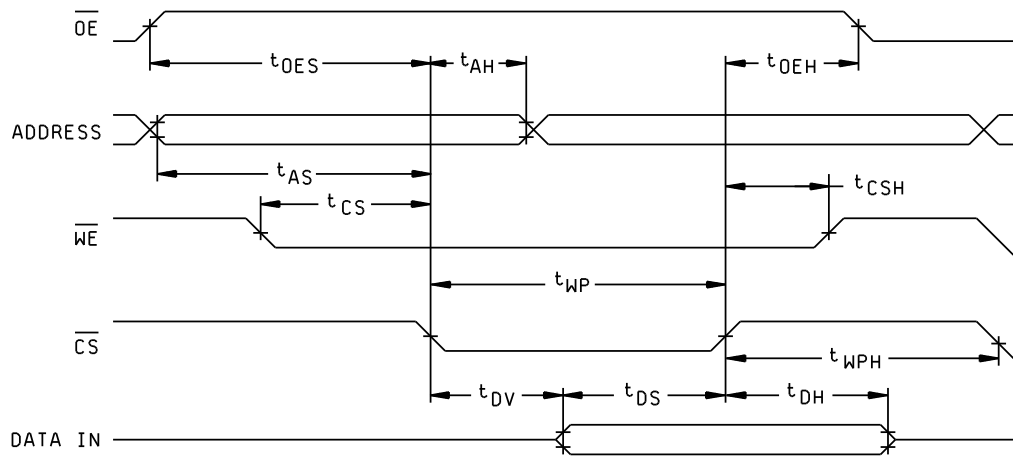
STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
13



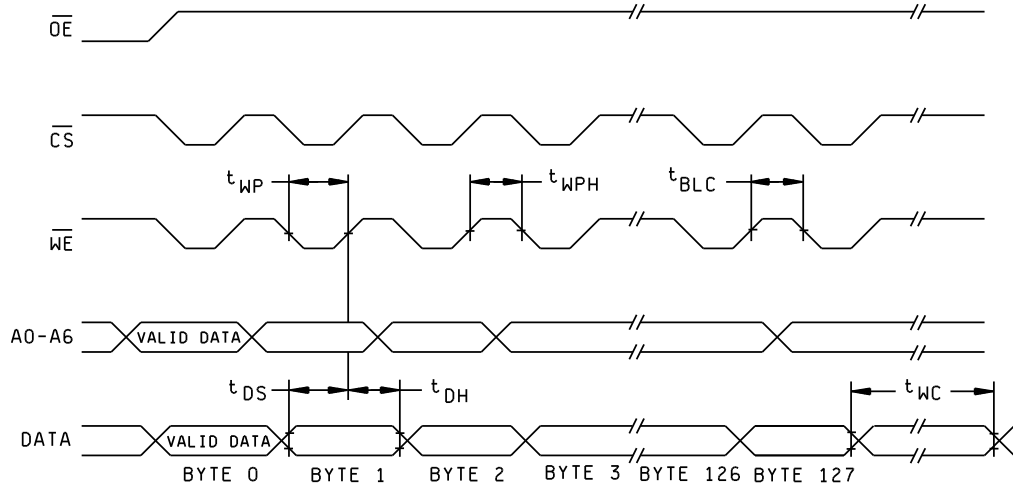
NOTES:

1. A write cycle is initiated when \overline{OE} is high and \overline{WE} or \overline{CS} is pulsed low when \overline{CS} or \overline{WE} is low. The address is latched on the falling edge of \overline{WE} or \overline{CS} , whichever occurs first. In either case, the address setup requirement applies to the falling edge of \overline{CS} due to the inclusion of an address decoder in the device.
2. Due to the inclusion of the address decoder in the device, the \overline{WE} and \overline{CS} write control timings will vary. When utilizing the \overline{CS} controlled write operation, all hold timings must be extended by the 25 ns propagation delay of the address decoder. For a \overline{WE} controlled write operation, \overline{CS} must be a minimum of 125 ns to accommodate the additional setup time required.
3. The delay required from the previous write operation to the next must be a minimum of 10 μ s.

\overline{CS} controlled

FIGURE 5. Write cycle timing diagram - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 14



NOTES:

1. A17 and A18 are used to select one of four separate blocks within the device.
2. A7 through A16 are used to specify the page address and must be the same throughout a single page mode write.
3. A0 through A6 are used to address specific bytes within a page.
4. Parameter t_{WC} is the write cycle time which will begin 150 μ s after the last byte has been loaded.
5. A write cycle is initiated when OE is high and WE or CS is pulsed low when CS or WE is low. The address is latched on the falling edge of WE or CS, which ever occurs last. In either case, the address setup requirement applies to the falling edge of CS due to the inclusion of an address decoder in the device,(See figure 5).
6. The delay required from the previous write operation to the next must be a minimum of 10 μ s.

FIGURE 6. Page mode write timing diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 15

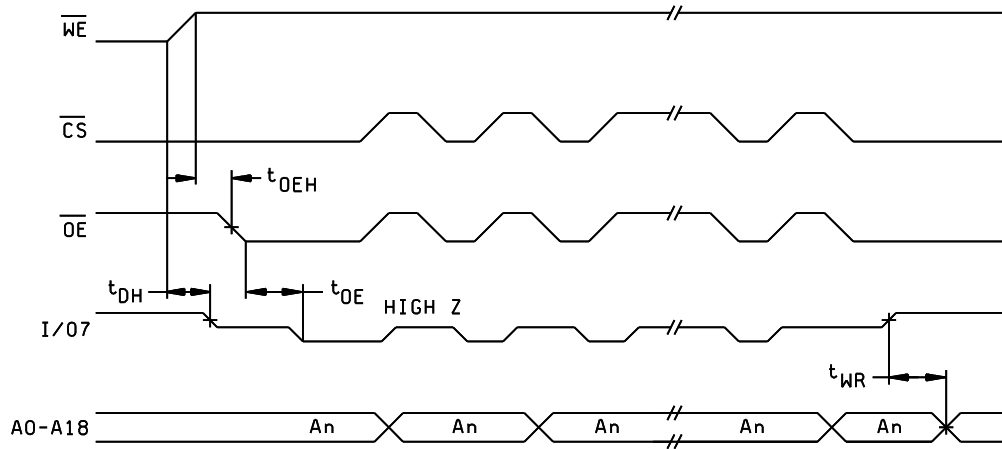


FIGURE 7. Data polling AC timing diagram.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
16

Device type 05 only

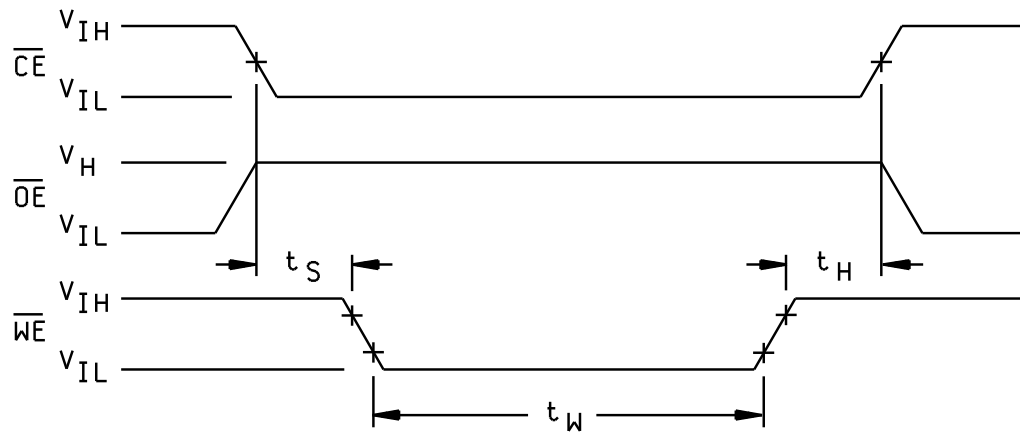


FIGURE 8. Chip erase waveforms.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
17

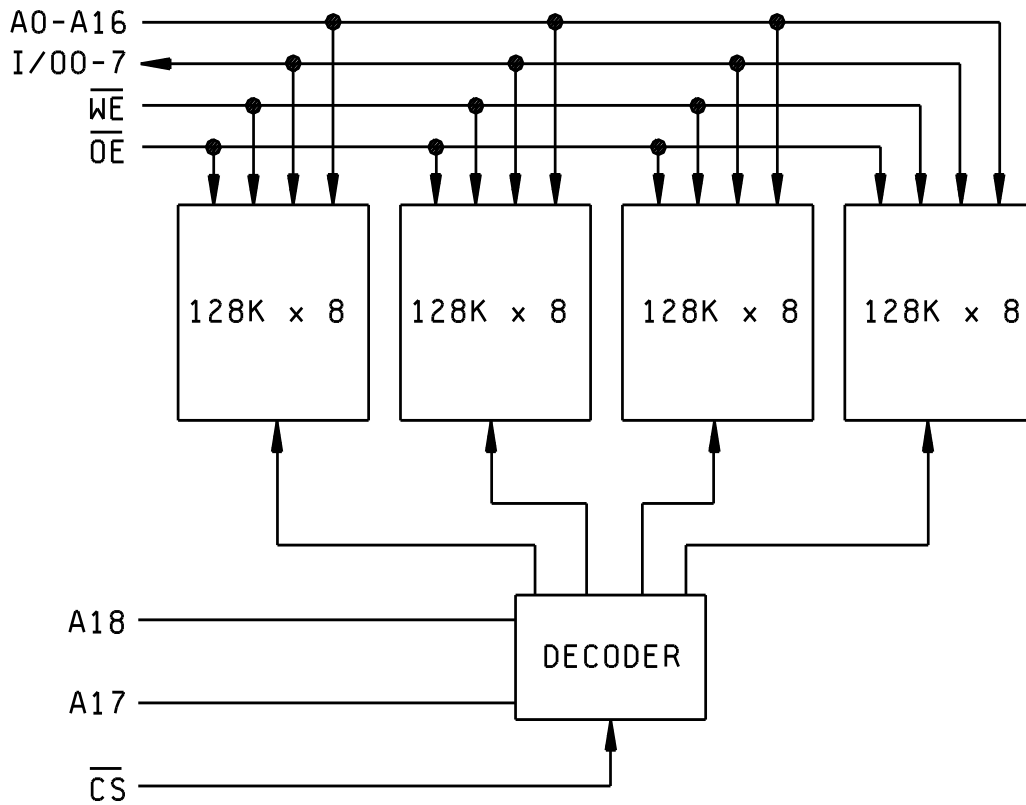


FIGURE 9. Block diagram.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93091

REVISION LEVEL
B

SHEET
18

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EL or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.
 - (3) Prior to burn-in all devices shall be programmed with a 00 hex data pattern to the entire memory array. The resulting pattern shall be verified before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall not be delivered.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 shall be omitted.
- c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.
- d. The following data patterns shall be verified during subgroups 7, 8A, and 8B:
 - (1) 0's to all memory cell locations.
 - (2) 1's to all memory cell locations.
 - (3) Checkerboard pattern to entire memory array.
 - (4) Checkerboard compliment to entire memory array.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. All devices requiring end-point electrical testing shall be programmed with a checkerboard pattern of alternate rows of AA hex and 55 hex.
- c. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EL or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 - (4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 19

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 9
Final electrical test parameters	1*, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group A test requirements	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
MIL-STD-883, Group E end point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.

** When applicable to this standardized military drawing,
the subgroups shall be defined.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table II herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5$ percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 20

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EL, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EL, Dayton, Ohio 45444, or telephone (513) 296-5373.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-PRF-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-PRF-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-HDBK-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-HDBK-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-HDBK-103	MIL-HDBK-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DESC-EL and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93091
		REVISION LEVEL B	SHEET 21

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-04-22

Approved sources of supply for SMD 5962-93091 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EL. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-9309101HXX 5962-9309101HYX	54230 54230	WE-512K8-150CQ WE-512K8-150CQ
5962-9309102HXX 5962-9309102HYX	54230 54230	WE-512K8-300CQ WE-512K8-300CQ
5962-9309103HXX 5962-9309103HYX	54230 54230	WE-512K8-250CQ WE-512K8-250CQ
5962-9309104HXX 5962-9309104HYX	54230 54230	WE-512K8-200CQ WE-512K8-200CQ
5962-9309105HYX	54230	WE-512K8-200CQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

54230

Vendor name
and address

White Microelectronics
4246 East Wood Street
Phoenix, AZ 85040-1943

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.