

MEASUREMENT OF SINGLE EVENT EFFECTS IN THE 87C51 MICROCONTROLLER *

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*Abstract**

This report presents the results of Single Event Effect (SEE) characterization testing of the Intel 87C51FC microcontroller for use in Space Station Freedom (SSF). The 87C51FC exhibited 4 types of SEE: RAM upset and three types of system errors, i.e., reset, latchup, and power cycle (a condition not correctable by the onboard watchdog timer). The microcontroller cross sections and response rates for these single event effects were determined.

I. Introduction

Space Station Freedom had intended to use the 87C51FC microcontroller extensively in the Data Management System and other subsystems. In view of the demonstrated susceptibility of similar Intel microprocessors, (e.g., the 80386 [1] and the 80C186 [2]) the 87C51FC was identified early as a prime candidate for SEE testing.

As a part of Boeing's overall task, we conducted single event effects tests on the 87C51FC microcontroller to determine the cross section and response rate for SEE, such as upset and latchup. The same basic experimental apparatus was used for all tests and the tested parts were exposed to heavy-ion beams and beams of energetic protons. The response rates of the microcontroller were calculated using the galactic cosmic ray (GCR) and trapped proton environments defined for SSF [3].

Data were also taken for the 87C51FB microcontroller. These SEE data are not presented here but are available in the full report [4].

SEE testing of microprocessors has been carried out extensively over the years [5-9]. Koga [7] defined several scenarios for microprocessor tests. This research described in this paper used a technique that may be roughly classified as the "Self-testing Single Computer Method". One of the relevant differences between the 87C51 and a microprocessor is the large amount of on-board RAM in the microcontroller. This lessens the relative impact of register upsets, which Koga

stated may "overestimate the device upset rate by as much as an order of magnitude". Here, the predominance of RAM over registers allowed for useful device upset estimation.

Preliminary testing of the 87C51FC was carried using the University of Washington Tandem Van de Graaff. (Reference [10] gives a brief description of the facility and procedures used there.) There, upset and latchup were observed as well as several new effects described in this report.

Further testing was conducted at three separate facilities: a) the 88-inch cyclotron at the Lawrence Berkeley Laboratory (LBL) for the heavy-ion tests, b) the Harvard Cyclotron Laboratory (HCL) for protons with energies of up to 148 MeV, c) the Tri-University Meson Facility (TRIUMF), for protons with energies of 200 MeV and 500 MeV.

The Intel 87C51FC is a highly integrated 8-bit CMOS III-E microcontroller based on the Intel MCS-51 architecture and is optimized for control applications. The FC version has 32K-bytes of on-chip EPROM. It has 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. Additional features of the microcontroller, common to both versions, include: a) four 8-bit bi-directional parallel ports, b) three 16-bit timer/counters, c) programmable counter array, d) full-duplex programmable serial port, e) interrupt structure, and f) power-saving modes.

2. Test Environments and Dosimetry

A. LBL 88-inch Cyclotron

Tests at the LBL 88-inch cyclotron used the "Aerospace Cocktail" [7,11]. This consisted of four different heavy ions (Kr, Ne, Ar, N), all with an energy per nucleon of 4.5 MeV/amu (atomic mass unit). In addition, the cyclotron was retuned to provide nitrogen ions at a higher energy (7.9 MeV/amu) for a lower LET (linear energy transfer).

The Boeing SEE test chamber was attached directly to the beamline and contained the device under test (DUT) mounted on a test circuit card. The card and DUT were installed on an apparatus that allowed rotation of the card and DUT with respect to the beam line. Tests were conducted at multiple angles to obtain finer adjustment of LET. To a first

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approximation, effective LET increases with increasing angle as given in equation 1. (Exposure at angle also modifies the effective incident fluence).

$$LET_{eff} = \frac{LET_{normal}}{\cos q} \quad (\text{Eq. 1})$$

$$f_{eff} = f_{normal} \cdot \cos q$$

The ion exposure environments and the corresponding linear energy transfer values are listed in table 1.

Ion	Energy MeV	LET MeV-cm ² /mg	R(Si) μm	Flux Ions/ cm ² /sec
Kr	380	38.5	46	2E2
Ar	180	14.3	47	5E2
Ne	90	5.5	54	7E3
¹⁵ N	67	2.8	70	2E4
¹⁴ N	110	2.0	150	2E4

Table 1 Heavy Ion Beam Characteristics. LET's and ranges are for normal incidence. Flux values are approximate.

The temperature of the DUT within the test chamber was controlled and monitored using a Boeing designed system including electrical heating elements and temperature sensors that were attached to the DUT using thermal grease.

On-line dosimetry for each run was based on the reading of a PIN diode located just upstream of the DUT location. The use of a PIN diode for on-line flux monitoring of heavy-ion beams is a common technique, previously described in reference [12]. The beam flux was adjusted with attenuators to achieve one or two upsets per time frame (see section 4.A for a description of time frames). Heavy-ion fluxes were variable, typical values being given in table 1.

B. Harvard Cyclotron Laboratory Cyclotron

Tests at the Harvard cyclotron used proton beams of five different energies: 20, 40, 70, 110, and 148 MeV. The microcontrollers were exposed to fluences ranging between 1E10 to 5E10 p/cm² during the runs. The cyclotron produces protons of 160 MeV. Protons of lower energy were obtained by means of Lucite and lead degraders that also served to spread the beam. The HCL has developed an absolute dosimeter for its proton radiation therapy work [13,14] and this was used for these tests. Beam size and uniformity were determined with exposures of Polaroid film and were observed to vary no more than 10% across the exposure area as defined by a collimator.

C. Tri-University Meson Facility

Tests at TRIUMF used proton beams of 200 MeV and 500 MeV. The microcontrollers were exposed to fluences ranging between 1E10 to 5E10 p/cm² during the runs. The beam was collimated using a series of collimators arranged to provide a 2.5 x 5.0 cm aperture. This allowed beam illumination of the DUT and not the supporting devices on the test circuit card. A

small scintillator was used to scan the beam and determine beam uniformity (down less than 20% at the edge).

3. Test Approach

Microcontroller upsets are expected to fall under two general categories: data upsets and functional upsets. Data upsets are upsets that occur in RAM, counters, or shift registers, and certain SFR's, which can be detected by the microcontroller executing a test program and which are reset under test program control. Functional upsets are upsets of internal nodes, such as the program counter (PC), special function registers (SFR's), program status register (PSR), or the program stack, which may affect program sequence. Functional upsets were usually more deleterious and required an external reset of the microcontroller to restore operation.

The intent of the test program was to exercise and check for the proper operation of the majority of the chip functions in such a manner as to measure the sensitivity of the devices to SEE. The test program was designed to initialize the test sample upon start-up or reset, and to continuously test the contents of internal storage registers and RAM. The program provided status signals to external instrumentation, which indicated device status and general failure modes. The internal storage structures, which were tested for data upsets, included: direct RAM, 64 bytes; indirect RAM, 128 bytes; serial-port shift registers, 16 bytes; and special function registers, 150 bits.

Since the microcontroller is in essence a complex state machine, certain internal storage nodes could not be tested explicitly. An upset in these areas could only be inferred from externally observable anomalous behavior, such as halting the program execution, program "run-away", or other behavior inconsistent with proper program execution. These conditions are described as latchup, power cycle or reset (lockup or runaway) depending on their effect and how proper microcontroller recovery was achieved. Detection of these conditions is described below. Data upsets were disregarded when reset or latchup conditions were detected.

A. Test Program Operation

The test program was constructed as a continuously repeating loop. On each pass the following chip areas and functions were examined:

- a) directly addressable RAM (DRAM),
- b) indirectly addressable RAM (IRAM),
- c) UART operation,
- d) the majority of the SFR's, which control the hardware operational states.

Port 1 on the microcontroller was used as the interface with external instrumentation to provide status and error information. The port lines were defined as follows: System_Boot (which was pulsed once as the device was reset); Loop_Start (which was pulsed at the start of each loop

iteration, indicating proper operation); Direct_RAM_Error, Indirect_RAM_Error, and SFR_Error (these were pulsed once for each failing byte in the tested area of the corresponding areas). RAM upset data, such as address and register contents, were also captured using a logic analyzer.

RAM, Serial port registers, and SFR were each tested with individual procedures. In this test approach all unused, contiguous memory blocks were filled with NOP's ending in a jump-to-self instruction. If a device upset were to occur which resulted in the program counter entering this unused space, control would eventually come to the jump-to-self instruction. After a maximum of 20 ms the external watch dog timer would initiate a reset, starting the program over.

B. Test Hardware

Control and monitoring of the microcontroller during test was accomplished with circuits on a test card, a latchup aid/power supply, and external test instrumentation. An Intel 87C51 evaluation board [15] was also used.

During normal microcontroller execution, the test program operated as a continuous loop, testing RAM and various internal nodes, and issuing a re-initialization signal to the "watchdog timer" (WDT) once every loop. (Koga, et al, [7] also used a WDT in their testing.) If no upsets were detected, a WDT re-initialization signal was generated by the test program before the program loop execution timer (PLET) timed out (approximately 20 ms). Time-out of this timer was indicative of anomalous program operation.

The WDT circuit consisted of three timers and a DUT power control circuit. The timers were: 1) the PLET, 2) a reset pulse-width timer, and 3) a power-down interval timer. When the PLET timed out, a signal was sent to the reset pulse-width timer and the microcontroller was reset (warm boot). This operation also reinitialized the PLET. If the microcontroller did not respond appropriately to the reset signal within a second time-out period, a power cycling sequence was initiated (cold boot). The power cycling circuitry removed power from the test device for approximately 10 ms. External scalars totaled the number of resets and the number of power cycling occurrences.

The microcontroller is also susceptible to single event induced latchup. Latchup conditions were detected with the Boeing designed latchup test aid (power supply, comparator, and power cycling circuitry), which monitored the supply current (I_{DD}) drawn by the microcontroller and cycled power to the circuit when latchup was detected. This test aid had been designed and developed to compare the supply current (nominally 20 mA) with a preselected trip level (50 mA), generate a signal to be recorded as a count in the latchup scalar when I_{DD} exceeds the trip level, and cycle power to the circuit so that proper operation is restored.

4. Test Results

A. Data Acquisition

Single event effect testing of random access memories is usually straight forward. A pre-selected pattern is recorded into the RAM that is periodically compared with the initial pattern as the device is exposed to a beam of ions to detect any upsets. Upsets may be counted with no regard for spurious events other than latchup so that the data resulting from these tests can be directly interpreted.

The procedure for taking upset data with the 87C51FC microcontroller is very different from such simple RAM's. First, the microcontroller has many different upset mechanisms, all of which must be taken into consideration and counted. Second, the microcontroller may generate a large number of spurious upsets caused by internal system upsets and these must not be counted with RAM upsets. Third, the microcontroller may stop functioning and require rebooting by a watchdog timer. During system reboot, spurious upsets were disregarded.

Additional failure modes were also discovered during the course of testing. It was determined that the watchdog timer circuit was not always able to reset the microcontroller. To alleviate this, occurrence of a second, consecutive, watchdog time-out caused the power to the microcontroller to be cycled. These events were accumulated in a scalar as "power cycle" counts.

Single event latchup events were detected by the increase in power supply current that they induced. The DUT power was cycled to correct the latchup condition and the number of these events was counted separately.

Upsets in the IRAM and DRAM segments of the microcontroller memory were detected by the running program and indicated by toggling discrete lines from the microcontroller. These were accumulated by scalars along with other signals from the system, described elsewhere. Diagnostic information (time and beam fluence) was recorded on other scalars.

Data Frames: The data acquired in the scalars was read by a computer at fixed time intervals. The scalars were then automatically reset and restarted. The advantage of this approach was that confined spurious counts to one "frame" of data and avoided contaminating the entire data set. At LBL, the data rates were high enough that data was taken every second, while at HCL and TRIUMF the upsets occurred less frequently, so the data frame was 10 seconds long.

B. Data Analysis

The accumulated data sets are quite voluminous. Each of the 200 or more runs consisted of up to 200 data frames of 10 scalar values of 7 digits each. Each frame of data was

analyzed by a set of automated spreadsheet macros and summed as described below for each different effect.

Latchup: The latchup events were detected by a current monitor after which DUT power was cycled to remove the latch condition. All data frames were counted toward the latchup total. The cross section was then just the total number of latchup events divided by the total fluence (corrected for angle and calibration factor). As expected, a latchup condition caused all of the other systems to generate spurious counts.

Power Cycle: A power cycle was defined as a condition not reset by a watchdog timer reset. It was detected by two sequential WDT time-outs. This situation was recovered by cycling the power to the DUT. All data frames that do not include latchup events were summed for power cycle data and fluence. Power cycle also caused the remaining signals to generate spurious counts.

System Reset: System reset was defined as a condition causing the watchdog timer to time-out and generate a reset/reboot signal. All data frames that do not include power cycle or latchup events were summed for system reset and fluence. System reset caused the remaining (RAM) signals to generate spurious counts.

IRAM & DRAM: All data frames that do not include system reset, power cycle or latchup were summed for IRAM and DRAM data and fluence. (In some instances, a large number of RAM upsets occurred in a single "valid" frame, these were presumed to be caused by "spill-over" from adjacent frame resets, latchup or other cause, and were not counted.) IRAM data was taken from upsets in 128 bytes (1024 bits). DRAM data was taken from upsets in 64 bytes (512 bits). The RAM bit upset cross sections (number of upsets divided by effective total fluence) were obtained by dividing the cross section by the number of bits.

Data Subsets: The plotted data was obtained by summing subsets of data. Many independent variables were tested for effect: i.e., bias voltage, DUT temperature, device type (FB or FC), and device serial number. Some variables were seen to be important for some effects: voltage and temperature on latchup [11], and voltage on upset, for instance. However little variation was seen for other variables and effects, such as temperature on upset. In addition, little device-to-device variability was seen. Such data was then summed for such subsets to reduce the statistical errors.

C. Heavy-Ion Cross Section Results

The results of heavy-ion testing are discussed for each observed effect in the following sections.

IRAM and DRAM: It was seen that the IRAM and DRAM bit cross sections for single event upset are essentially identical, so only IRAM data is presented in figure 1. This was not

unexpected since the IRAM and DRAM are composed of the same kind of RAM cell.

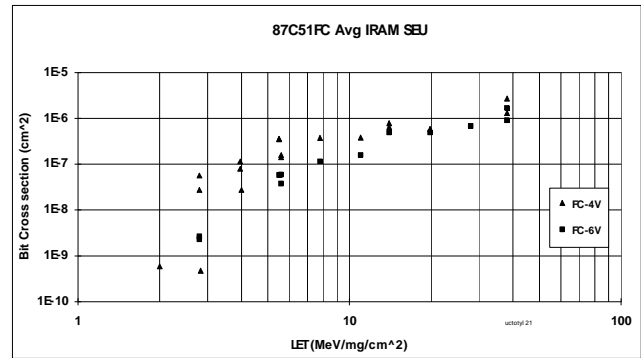


Figure 1 - Average IRAM Cross Section. Bit upset cross section for 87C51FC "IRAM" versus LET. Data are shown for 2 voltages (4V & 6V).

It can be seen that the RAM upset cross section for the 4 volt bias condition is usually worst case, as expected. At low LET values, the difference between 4 and 6 volts can be more than an order of magnitude. At higher LETs the difference is less. The device upset cross section is application dependent and is here defined as worst case, where all bits of IRAM, DRAM, SFR's, and other internal registers add up to approximately 2300 bits.

A logic analyzer was used to record data to investigate the distribution of errors over RAM address space, the occurrences of multiple bit errors, and the characteristics of error transitions. Histograms of memory errors showed no apparent trend, the error distribution seemed to be random over the address range. Error data was also analyzed to determine the number of multiple bit errors within a single word and to determine a preference of low-high or high-low transitions. For the logic analyzer errors that were processed, the percentage of multiple bit errors was seen to be approximately 2%. High-to-low error transitions showed a pronounced preference (accounting for 75% of the RAM errors).

Special Function Registers: Limited data was taken for the special function registers (SFR's). The data is similar to the RAM data and so is not presented.

System Lockup/Reset: The device cross section for "system lockup/reset" is shown in figure 2. It can be seen that the shape of the cross-section curve is similar to that for RAM upset. The ratio of device reset to RAM bit upset is plotted in figure 3. It can be seen that the ratio is nearly independent of LET at a value of about 100 RAM bits per device reset. This leads us to presume that the cause of system reset is a subset of RAM upsets. Possible candidates for inducing reset are upsets of the program counter or other registers (SFR's) or upsets of data stored in the program "stack". A rough calculation of the number of such bits was done and seen to be close to what was observed. It is expected that this value is very application

dependent. A program that uses a large amount of "stack", for instance, would likely have a higher reset ratio.

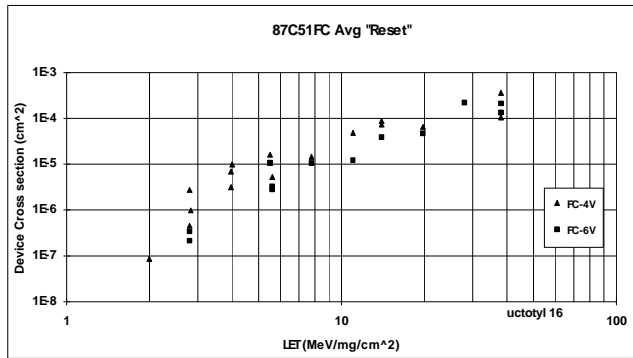


Figure 2 - Average Reset Cross Section. Average device "Reset" cross section for 87C51FC versus LET. Data are shown for 2 voltages (4V & 5V).

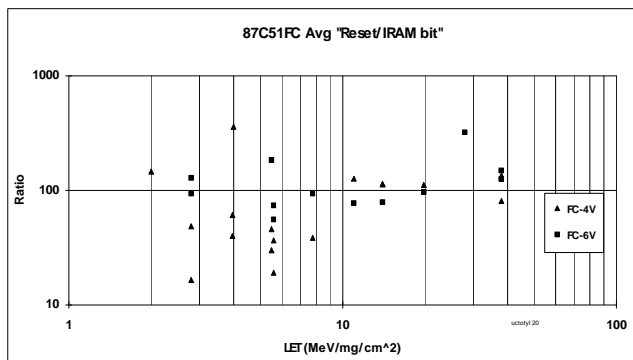


Figure 3 - Reset/IRAM Ratio. Average ratio of "Reset" to RAM Bit versus LET. Data are shown for 2 voltages (4V & 5V). It can be seen that the ratio is approximately constant.

Latchup: The single event latchup data is shown in figure 4. It can be seen that the 6-volt data at high temperature is worst case, as was expected [11].

The device current was monitored during irradiation to krypton ions and collected for successive latchup events. Latchup current was recorded each time there was a change. Two different tests were conducted. In figure 5, the individual current increases are depicted in histogram fashion (as was also done by LaBel, et al [9]). The normal operating current was 20 mA and our latchup detection circuit triggered at 50 mA, a threshold of 30 mA. The detection threshold is indicated in the figure and it can be seen that we detect approximately 90% of all latchup events (with substantial variability). The remaining 10% of sub-threshold, undetected upsets were probably the high LET "power cycle" events described below.

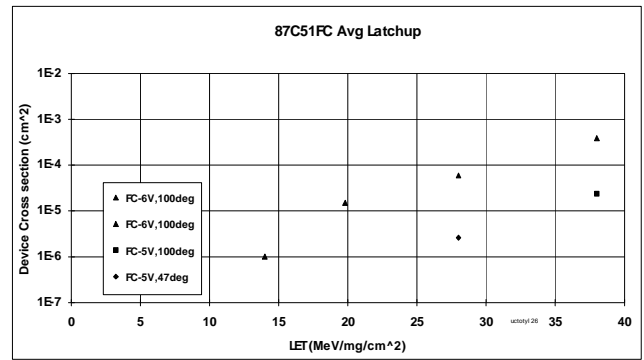


Figure 4 - Average Latchup Cross Section. Device latchup cross section for the 87C51FC versus LET. Data are shown at 5 & 6V and at 47 & 100^o C.

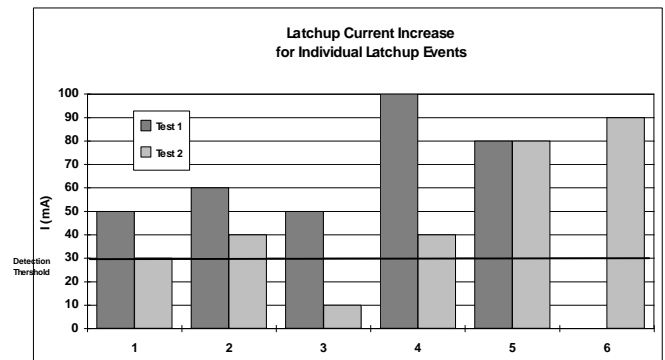


Figure 5 - Latchup Current Histogram. Individual latchup current increments for several SEL events. The latchup detection threshold is indicated.

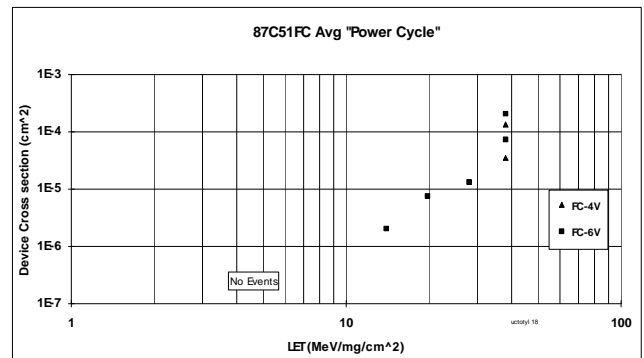


Figure 6 - Power Cycle Cross Section. Cross section for "Power Cycle" versus LET. See text for further details.

Power Cycle: The cross section for "power cycle" events is shown in figure 6. In this figure the caption "No Events" indicates the detection limit for the fluence of the run (i.e., 1/fluence). The high cross section for the 6-V high-LET data suggests a latchup related effect. Indeed, the cross section is approximately what one would expect from undetected latchup (see discussion of latchup above).

D. Proton Cross Section Results

The low LET threshold seen in heavy-ion tests indicated that the 87C51FC would also be upset by trapped protons [16,17]. Proton SEU tests were thus conducted on the 87C51FC microcontroller at both HCL and TRIUMF.

Upsets were encountered in all of the proton SEU runs but proton-induced latchup was not. The fact that no latchup was measured is consistent with the findings of other workers. Earlier this year researchers at JPL [18] and ESA [19] reported on proton-induced latchup measurements. In both cases the susceptible parts had a heavy-ion LET latchup threshold of approximately 3 MeV-cm²/mg. Since our LBL tests on the 87C51FC microcontroller indicate a LET latchup threshold of greater than 10 MeV-cm²/mg that is considerably higher than 3 MeV-cm²/mg, it is not all surprising that no proton-induced latchup was recorded.

In general, we saw little variation in the number of upsets for the two temperatures (as was also the case for the heavy ion data). A parameter that was varied and which did cause a variation in the upset response was the bias voltage. The nominal bias voltage for the microcontroller is 5 volts. During the HCL tests, runs with 148-MeV protons were made with the bias voltage at 4.5 volts and 5.5 volts. As expected, the upset cross section at the lower voltage was greater, in this case about 30%, than at the higher voltage. The TRIUMF tests were conducted at 5 volts and 4 volts with the 500 MeV beam and only 4 volts with the 200-MeV beam. The combined upset cross section with 500-MeV protons is approximately 2.5 times larger at 4 volts than it is at 5 volts. To utilize all the proton SEU data, we have adjusted the data up or down to a bias voltage of 4.5 volts as shown in figure 7. Total dose effects were seen in the HCL and TRIUMF proton tests. The effects were small and were included in the analysis.

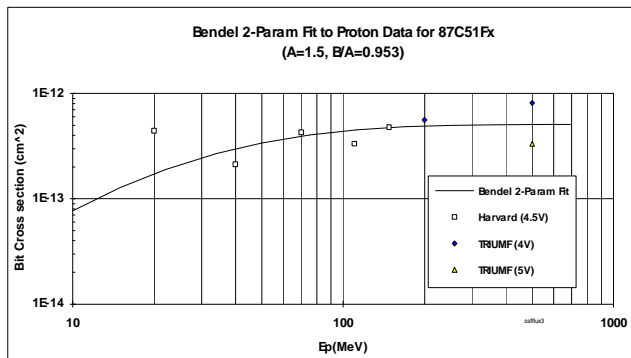


Figure 7 - Proton Induced SEU Cross Section and Fit. Proton bit upset cross section data taken at various facilities is shown versus proton energy. A 2-parameter Bendel fit is also drawn.

Figure 7 also shows a curve that is fit to 4.5-volt data points. The 2-parameter Bendel model [20] has been suggested for proton SEU cross sections and is given by:

$$S = \left(\frac{B}{A}\right)^{14} \cdot \left[1 - e^{(-0.18 \cdot \sqrt{Y})}\right]^4 \times 10^{-12} \text{ cm}^2 \quad (\text{Eq. 2})$$

$$Y = \sqrt{\left(\frac{18}{A}\right)} \cdot (E - A)$$

where: E = proton energy
A = 1.5
B/A = 0.953

The agreement between the data points and the fit is adequate. However, while the Bendel model expects the upset cross section to decrease at low energies, our data indicates no fall-off. The 20 MeV data point has a large energy uncertainty, however, since more degraders were used to achieve this low energy.

E. Heavy-Ion Rate Results

Rate predictions for heavy-ion SEE (for the worst case operation) were made for the failure modes for the 87C51FC microcontroller. These were performed in accordance with procedures found in references [3] and [4] and used the galactic heavy-ion spectrum appropriate for the SSF orbit. Results are given in table 2.

Environment			
	GCR	Proton	P&GCR
Shield (mils Al)	100	150	N/A
σ_{asym} (cm ² /chip)	7.0E-3	1.0E-9	
E_{thresh} (MeV)	N/A	20	
LET_{thresh} (MeV-cm ² /mg)	2.5	N/A	
Upset Rate (per day)	3.2E-3	3.8E-3	
Mean Time to Failure			
Upset (Days)	320	260	140
Reset			10 Yrs
Latchup	630 Yrs		630 Yrs

Table 2. Rates for upset, reset and latchup for the 87C51FC microcontroller. Rates are based on worst case conditions (4V for upset and reset, 6V for latchup). Rate calculations use the environments and procedures found in reference [3].

The "reset" or "lockup" failure rate can be obtained by multiplying the bit upset rate by 100. It must be emphasized that this is very application dependent. The failure rate due to "power cycle" was always less than the latchup rate and may be an artifact of the test technique.

F. Proton Upset Rate Results

The proton upset cross section allows us to calculate the rate of upset induced in the 87C51 microcontroller by the trapped protons in the Space Station orbit. Using the two-parameter Bendel fit and the differential proton flux [3], the upset rate is also given in table 2.

G. Sensitivity Analysis

It is of interest to see to what extent our data is "complete" in LET or proton energy coverage. A sensitivity function can supply this information. The sensitivity function is simply the cross section times the appropriate spectrum plotted against LET or energy. (For a logarithmic X-axis, the sensitivity data is multiplied by the X-value.) This was done for heavy-ion data and is plotted in figure 8 for SEU and figure 9 for SEL. Proton RAM upset data is plotted in figure 10. It can be seen that all of the latchups resulted from ions at an LET where the data is good. The upset sensitivity is peaked between 2 and 4 MeV-cm²/mg; however, the worst case error is acceptable.

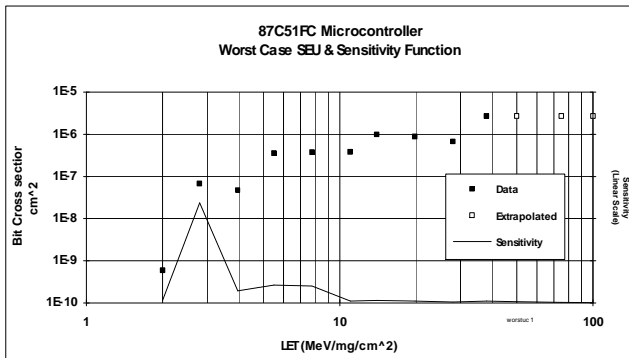


Figure 8 - SEU Sensitivity. The worst case heavy ion bit upset cross section is plotted together with the sensitivity function for the environment at low earth orbit.

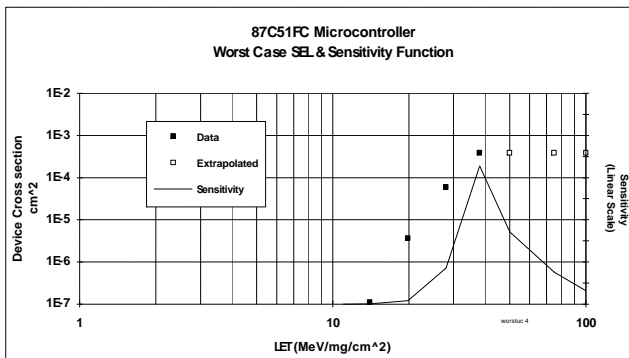


Figure 9 - SEL Sensitivity. The worst-case heavy-ion latchup cross section is plotted together with the sensitivity function for the environment at low earth orbit.

This sensitivity analysis establishes good confidence in the calculation of upset and latchup rates since most of the upsets and latchups were due to LETs and energies where the data is statistically significant and relatively few upsets were due to LETs and energies where the data is statistically marginal.

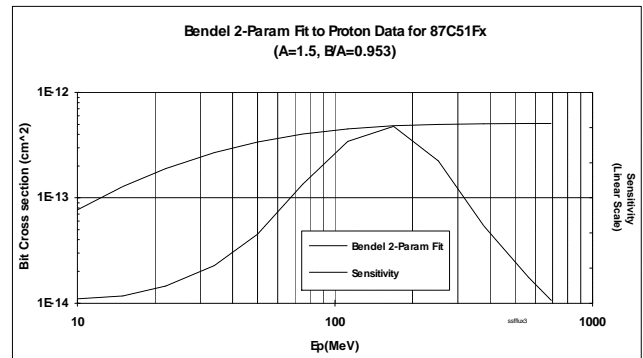


Figure 10 - Proton SEU Sensitivity. The proton SEU bit cross section is plotted together with the sensitivity function for the environment at low earth orbit. (FB & FC devices are averaged.)

5. Summary

Data upset, lockup/reset, and latchup rate predictions based on Space Station Freedom radiation environments and on test data for the 87C51FC microcontrollers are summarized in table 2. The upset rates are seen to be dominated by the proton environment.

These heavy-ion and proton SEE rates were found to be non-negligible for use in many SSF systems. Boeing chose to complete development and initiate production of a SEE-hardened [21] version of the microcontroller that is expected to be used in many of these systems.

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