Single Event Effects Testing of the Intel Pentium III (P3) Microprocessor

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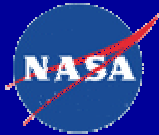**Ronald Stattel**
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Many future NASA missions will require extensive on-board computation capability which raises the issue of availability, cost and capability of radiation hardened or radiation tolerant microprocessor systems. Radiation hardened computer systems are often costly and are actually two or three generations behind in computational capability, a significant shortfall for missions that may require state-of-the-art (SOTA) capability.
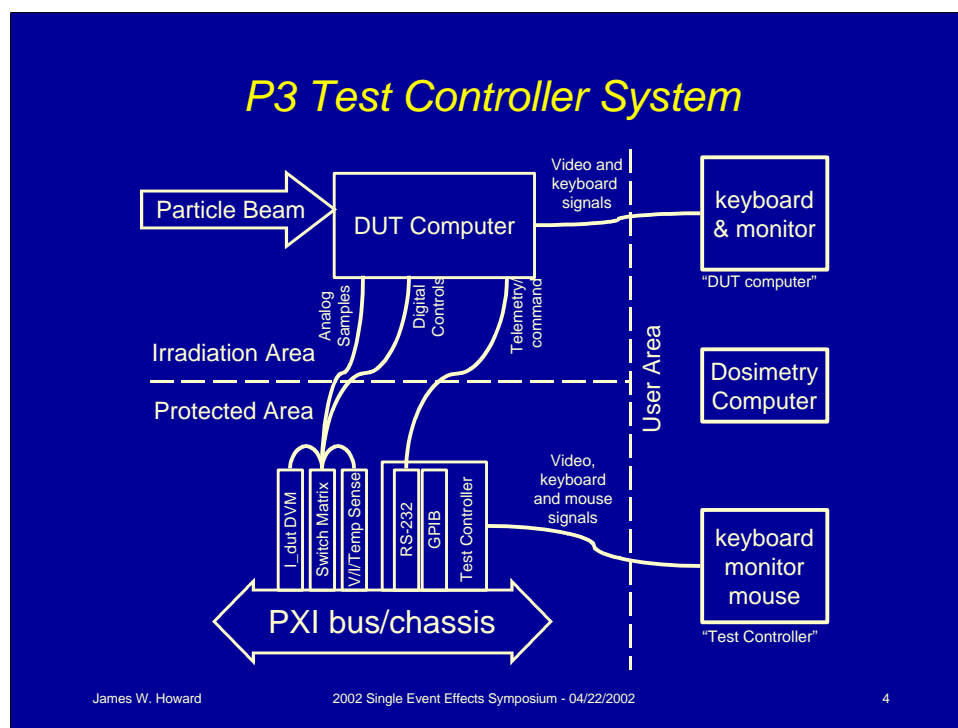
To confront these issues, NASA instituted the Remote Exploration and Experimentation Project (REE) with the goal of transferring commercial supercomputer technology into space using SOTA, low power, non-radiation-hardened, commercial-off-the-shelf (COTS) hardware and software to the maximum extent possible. Testing of the Pentium III microprocessor was done with this effort in mind.

Outline

- **Introduction**
- **Test Methodologies**
- **Hardware**
- **Software**
- **Test Issues**
- **Sample Data**
- **Summary**

Test Methodologies

- Single Event Effects
  - Architecture and technology implications
    - Test SOTA technology and exercise that technology
    - Exercise independent pieces of the architecture with maximum duty cycle
    - Investigate technology versus operational conditions (e.g., rated versus operation clock speeds)
  - System level impacts
    - Destructive events
    - Function interrupts vs. non-recoverable upsets vs. recoverable upsets

P3 Test Controller System

Particle Beam → DUT Computer

Video and keyboard signals → keyboard & monitor
"DUT computer"

Analog Samples | Digital Controls | Telemetry/command

Irradiation Area

User Area

Protected Area

Dosimetry Computer

I_dut DVM | Switch Matrix | V/I/Temp Sense | RS-232 | GPIB | Test Controller

Video, keyboard and mouse signals → keyboard monitor mouse
"Test Controller"

PXI bus/chassis

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The system hardware consists of two subsystems, the Test Controller and the DUT computer subsystems. The above figure illustrates the overall test configuration. The Test Controller hardware is based on the PXI specification. The PXI subsystem resides within the irradiation chamber but is removed from the DUT subsystem by more than 15 feet. It consists of the PXI components, the PXI Computer <-> DUT Computer cabling and the user interface.

The PXI components include the PXI chassis, which contains an embedded controller (running WinNT, Labview (LV) environment, and a custom LV application), a signal switch matrix, and two digital multimeters (DMMs) in the voltage measurement mode. The switch matrix provides two functions: The multiplexing of analog signals to one of the DMMs, and contact closures (pulling signal levels to ground). The other DMM is dedicated to monitoring one specific analog value and measuring that without regular periodically switching, so that it may measure more frequently with less delay.

The user interface for the PXI Computer, network connectivity (for data file access) and AC power feed are also components of the PXI Computer. An extended (via a CAT5 cable based extender from Cybex, Inc.) keyboard, monitor, mouse user interface provides user control of the PXI computer from the user facility. Most of the PXI Computer <-> DUT Computer cabling leaves the PXI subsystem from the switch matrix, exceptions are the AC power cable to power the DUT computer and a serial (RS-232) cable for telemetry/command of the DUT computer (telemetry originates within the DUT Computer, commands originate within the PXI Controller).

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P3 DUT Computer Test System
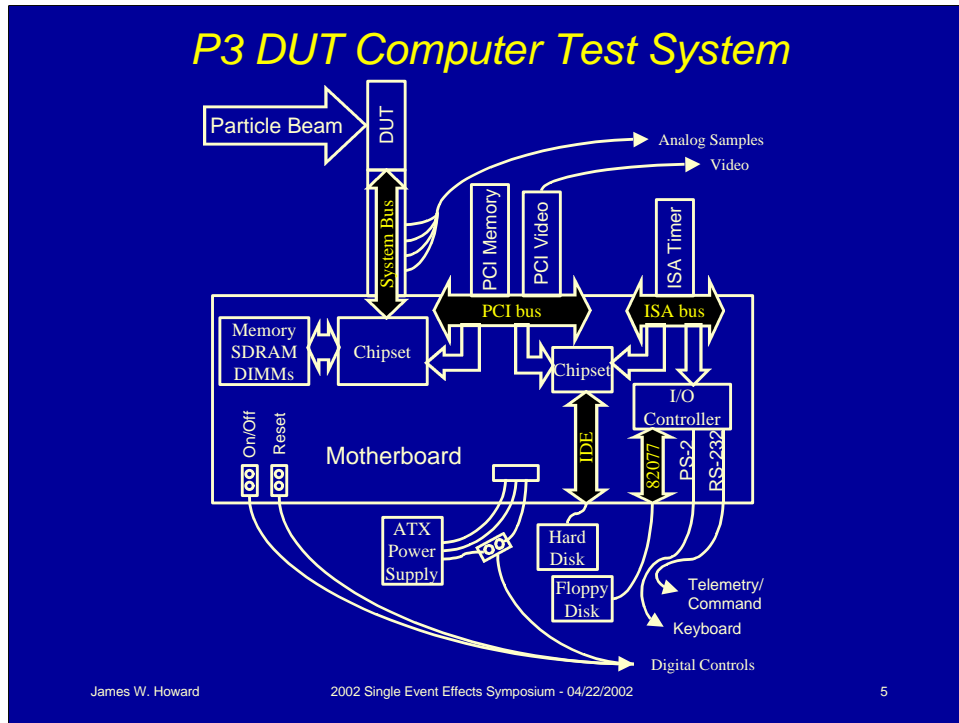
The DUT computer subsystem consists of the components immediately connected with the operation of the DUT computer, including components mounted directly to the motherboard, components located nearby (e.g. disk drives) and connected via cables, and the user interface.

Two different motherboard types were used (one for the SC-242 DUT and one for the FC-PGA370 and FC-PGA2 DUTs). Directly attached to one of these commercial motherboards are the modified P3 DUT processor (on top of a DUT processor extender card in the case of the SC-242 DUT), a RAM module (DIMM), the video, and a PCI-bus memory board (This board and the serial port are handed identical copies of the telemetry stream; the contents of the memory board will survive a soft reset of the DUT computer for later readout through the RS-232 port in case the RS-232 port crashes.).

The DUT computer motherboard resides in the test chamber, positioned directly in front of the particle beam but so that only the DUT processor is irradiated. A metal base with standoffs holds the SC-242 motherboard horizontally so that the DUT sits vertically, high on its extender board. Only the DUT and its cooling system are irradiated. In contrast, the FC-PGA370 motherboard sits vertically, with its "front" edge in an (insulated) slot cut into the aforementioned metal base, with the top stabilized by a hinged support, so that the DUT, which is plugged directly into the motherboard socket, is also vertical. The proton beam penetrates the DUT, its cooling solution, and the motherboard but no active components are affected.

The DUT software is compiled in Microsoft Visual C++ with a Pharlap Linker Add-in. The tests are written in a combination of C and assembly language. The software is executed using the Pharlap Real-Time Operating System. Pre-emptive task switching is turned off. The DUT communicates to the user through a VGA/keyboard interface and a serial port to the test controller system. All telemetry is echoed to a memory area that is not destroyed upon soft-reset or short power cycles. This memory is dumped through the serial port to the test controller after a reboot following a crash of the system. This is performed in an attempt to recover information lost due to the crash.

There are nine tests available for testing the Pentium III components. Each test sends a keep-alive at approximately a one hertz rate (0.1 Hz for test "H") and sends error results as they happen. One test is selected for each exposure to the beam and the software repeatedly performs the test until a pre-determined dose is reached or the software stops communicating to the user.

There are eight tests designed to exercise the various aspects of the CPU during SEE testing:

A: Register Test

B: Floating Point Unit Test

C: Memory/Data Cache Test - Sequential

D: Task Switching Test

E: Instruction Cache Test

F: Floating Point Unit Test (Operation Intensive)

G: MMX Test

I: Memory/Data Cache Test - Offset

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Test "A" checks the general-purpose registers of the CPU. There are eight general-purpose registers.

Test "B" checks the Floating Point Unit (FPU) with a maximum of data transfer to the FPU. A buffer is loaded with the arguments and expected results for the five operations tested (fadd, fsub, fmul, fdiv, and fsqrt).

Test C performs cache test. If the cache is on, then the cache is turned off, the memory is loaded with an incrementing pattern and the cache is turned back on before entering the test. The memory is checked word by word. After each word is checked, its value is changed to the bitwise complement of the baseline. If the value is not as expected then an error is reported and an attempt is made to reset the value to the baseline.

Test "D" launches seven subthreads each with a counter that is reset to zero. Each thread increments its counter if the counter is less than 11 and then passes control to the next thread. The main thread then checks after 50 milliseconds to see if all of the counters have reached 11. If not an error is reported to the user.

Test "E" runs through 16K of instructions repeatedly. The instruction sequence is to increment the eax register from 0 to 3 checking in between each increment to see if the value is as expected, then to decrement the eax register 3 times and check to make sure it returns to zero. Any errors are reported to the user and the cache is invalidated.

Test "F" checks the Floating Point Unit (FPU) with a maximum of operations in the FPU. A buffer is loaded with the arguments and expected result.

Test "G" checks the Matrix Math Extensions (MMX). A buffer is loaded with the arguments and expected results for the four operations tested (pxor, por, pmul, pmulh, padds, addps, divps, and mulps).

Test "I" performs an alternate cache test. The difference between tests I and C is that bits are swapped in the location used to access the memory/cache. This has two effects. First, the area of cache used is different for the 50% and 25% cases. In test C 50% case, a contiguous half of the cache is used while in test I 50% every other tag (a tag marks 16 words) in the entire address range is used. Similarly for the 25% case.
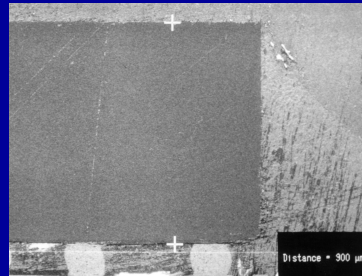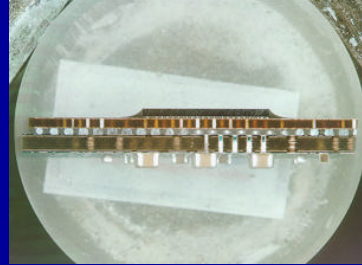
The data sets that are generated from Single Event Testing, due to the large test matrix, contain enormous amounts of data. It became necessary to generate software to deal with these large data sets to analyze the data under all the test conditions. A database form was chosen as the best form for this analysis. The database initially reads all of the test conditions, then allows to user to scan through the telemetry files. The user marks locations within the telemetry files with error annotations that are then stored in the database with those associated test conditions.

After each telemetry file has been annotated, the database can be queried via Structured Query Language (SQL) commands to extract only those conditions wishing to be analyzed. Depending on the detail of the SQL commands, either the event rate (or cross section) can be calculated directly or the selected data from the database can be exported in tabular format for other software to continue the analysis.

The Pentium III, when operating under normal conditions with the caches enabled, will draw in excess of 20 watts of power. If left in that state with no cooling, the processor will not even boot. Also, the Pentium III die, as procured as a COTS parts, are flip chip solder bubble bonded die to the DUT daughter cards. Since the beam must hit the die directly, the packaged heat sink and cooling fan must be removed. In its place a water-cooled jacket is used (thinned to 10 mils over the die for heavy ion testing).

The large thermal source is also the reason that the die cannot be thinned, as has been done with other flip chip parts. The thick substrate is the main thermal path for removal of heat from the junctions. Thinning this would place excessive thermal stresses on the die and most likely lead to structural failures.

With these parts being flip chip solder bubble bonded die, the sensitive regions of the processor approximately 900 microns deep in the silicon die with respect to the heavy ion incidence point. Thermal issues compound this by requiring cooling material in the beam line, as well. Therefore, only high energy and high Z beams are capable of penetrating and giving higher Linear Energy Transfer (LET) values in the sensitive regions.

If the beam energy is such that normal incidence the ions do not have penetration issues into the sensitive region but when the beam is either degraded in energy or the part rotated (to give a larger effective LET), there are penetration issues, then roll-off of the cross section curves may be observed. This would be seen as a high effective LET data point having a lower cross section than the previous lower effective LET point. For the beam used in this testing and the P3 die tested, this roll-off point is expected to occur somewhere between an effective LET of 10-20 MeV-cm2/mg.

What Have We Tested

- Intel Pentium III
  - Speed ranging from 550 through 1200 MHz
  - Represents 0.25, 0.18 and 0.13 μm technology
- AMD K7
  - Speeds ranging from 600 through 1000 MHz
  - Details of technology not available
  - High SEFI rates forced the removal of these parts from the study

Where Have We Tested

- GSFC TID Facility
  - Biased and Unbiased Co-60 Testing
- Indiana University Cyclotron Facility
  - Proton Displacement Damage
  - Proton SEE
- Texas A&M University Cyclotron
  - 55 MeV/amu Argon and Neon
  - LET range from approximately 3 through 15 MeV-cm^2/mg

TID/DDD Data

Pentium III DEVICE UNDER TEST (DUT) TABLE

Device	Rated Speed	Test Condition	Source	Exposure Levels (krads)
P3	800 MHz	Biased	Co-60	*511
P3	933 MHz	Biased	Co-60	573
P3	550 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	3700
P3	700 MHz	Unbiased	Co-60	336
P3	850 MHz	Unbiased	Co-60	697
P3	933 MHz	Unbiased	Co-60	2100

* Indicates part functionally failed

Dose Rate Biased - 2 rad(Si)/min
Dose Rate Unbiased - 7 rad(Si)/min

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Intel P3 parts were exposed to the total dose environment at the GSFC Radiation Effects Facility (Cobalt-60). The results of this testing are summarized in the above table. It should be noted that the one DUT rated at 550 MHz is 0.25 μm technology, while all other DUTs tested are 0.18 μm technology.

Several P3 devices, in an unbiased condition, have been exposed to various doses, one in excess of 3700 krads(Si). They have shown little sign of degradation in either supply currents or timing and functionality testing. Biased testing of one Pentium III DUT did functionally fail after exposure to an approximate dose of 511 krads(Si). A replacement part was tested under bias, and had exceeded a dose of 573 krads(Si) when it was removed from testing.
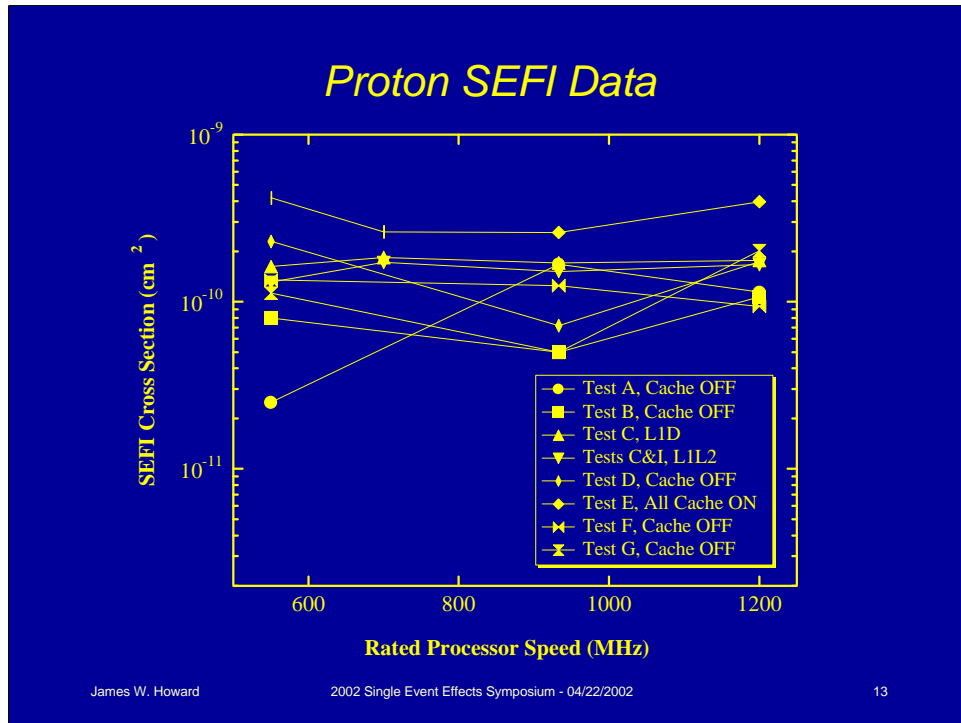
The above figure shows the Pentium III (P3) SEFI cross sections as a function of the DUT rated speed for all test software and conditions. For test software being executed, there is little, if any, dependence as all data lies within approximately one order of magnitude. However, the curve that is the highest (Test E) is also the case where the L1 instruction cache is enabled. It could be argued that the difference observed is real and that the L1 instruction cache being enabled will lead to more SEFIs, but the data does not show enough difference to say it is statistically significant. Also, no speed dependence is observed.
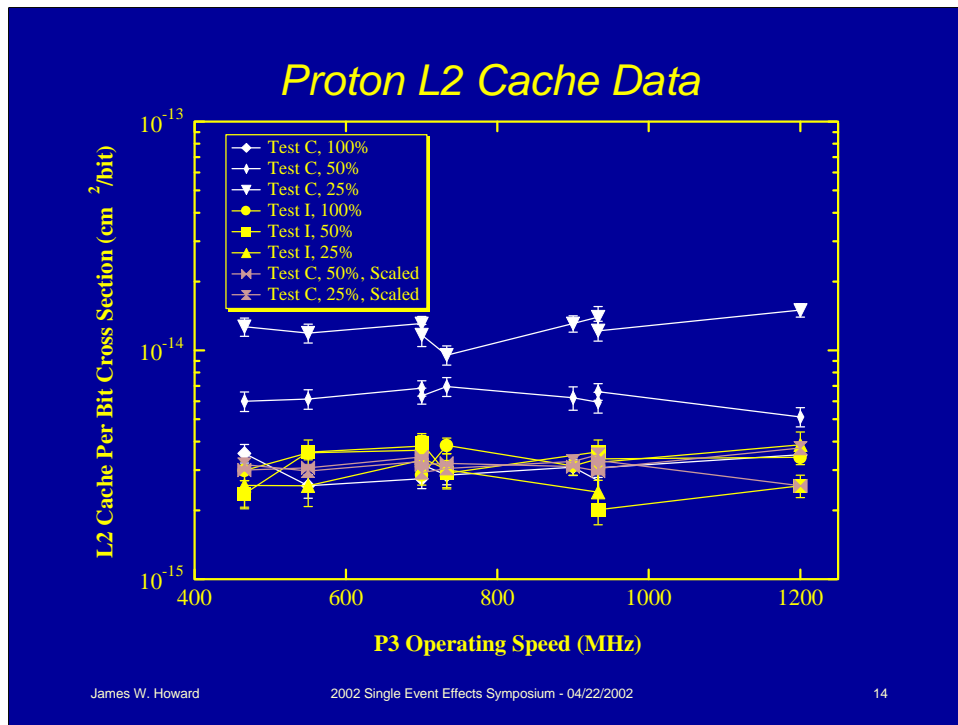
The data, shown in above figure, points out a major testing issue that arose during the last heavy ion test. The issue was that when test C was run for the 50 and 25 percent cases, a different per-bit cross section was seen. This same effect was seen in this proton test (the one-sigma error bars do not allow for the possibility of statistics being the cause). However, for this proton test, test I software was written to provide an alternative method of testing the L2 cache that forced a non-sequential addressing scheme. As can be seen, the three percentage cases for test I do not show the same variation as test C. In fact the three test I curves fall on top of the 100% test C curve, giving credence that the 100% test C data gives the correct data.

It is not clear what is causing this difference between test C and I. There is nothing in any Intel documentation that indicates any special data fetching, storages, etc., whenever data is continually fetched sequentially. Even is there was, that would not explain why the 100% case test C is unaffected by whatever mechanism is in place. Another observation that adds to the confusion is the data for all the per-bit cross sections for tag bits for all caches (L1 Data cache from test C, L2 cache from both test C and I, and L1 Instruction cache from test E) coincide. This would seem to indicate that the correct number of tags are used in each of the difference percentage cases in the sequential and non-sequential addressing tests, as their per-bit cross section are the same. With the correct number of tag bits being used, this definitively implies that the correct number of cache bits are being used.

This points out a major testing issue when dealing with a "black box" part such as the Pentium III. A lesson-learned from this is that the parameter space for a test such as this, needs to be broadened to allow for unknown effects to arise, be seen, and hopefully understood.

Proton Cache SEU Data

Summary Per Bit Cache Cross Sections						
Cache State	Single Tag Errors	Single TE Error	Multiple Tag Errors	Multiple TE Error	Cache Bit Errors	Cache BE Error
L1 Data	4.62×10^{-14}	2.23×10^{-14}	9.55×10^{-16}	4.78×10^{-16}	4.96×10^{-14}	7.16×10^{-15}
L2	5.72×10^{-14}	6.15×10^{-15}	1.08×10^{-15}	1.08×10^{-15}	9.86×10^{-17}	4.30×10^{-16}
L1 Inst.*	2.77×10^{-14}	4.09×10^{-15}	6.03×10^{-16}	6.03×10^{-16}	3.19×10^{-14}	1.77×10^{-15}

Calculated values based on percentage of tag versus cache bits.

To generate the numbers in the above table all DUTs tested, at all test speeds for the various test conditions were combined into the respective conditions (as all the data shown to date has shown no processor speed or part-to-part variation for the Pentium III devices). This table contains the data for tests C (ignoring the data for 50% and 25% L2 cache cases) and I. It shows the cache bits cross section, the cache tags cross section and a cache tag upset mode cross section that appears to be multiple bit upsets in the tags. Of interesting note is that this mechanism is only present for the L2 cache tags. It is possible that the mechanism exists for the L1 cache tags, as well, but due to the small size, did not manifest itself in this test. The table also contains the one-sigma Poisson error for each of these cross sections, as well.
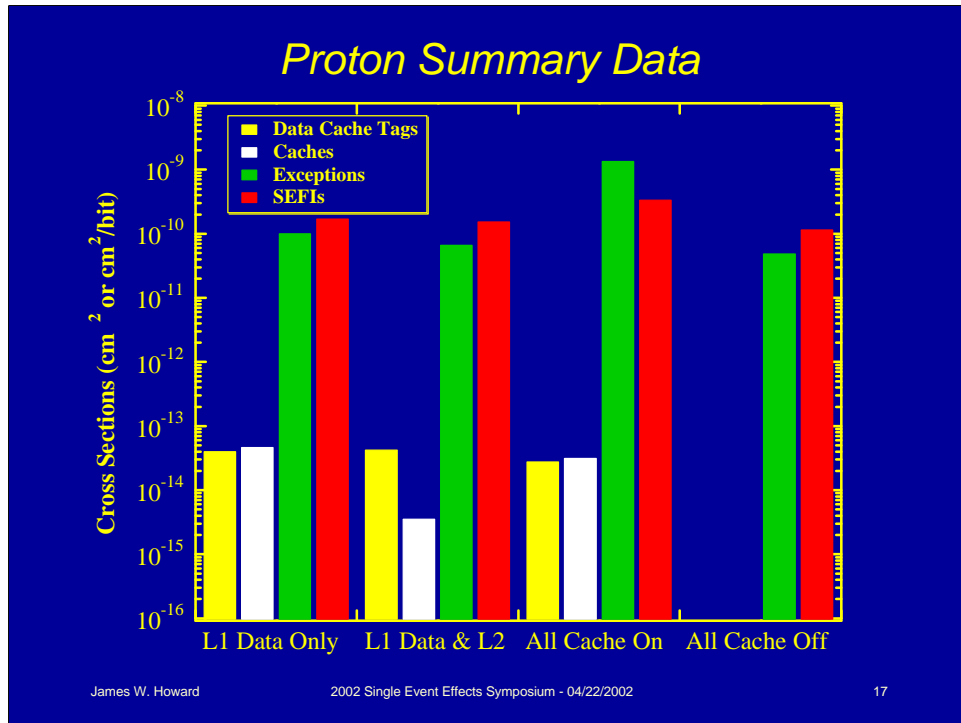
Proton Other SEU Data

| Total Cross Sections for Other Tests					
DUT	Test	Number of Upsets	Fluence (p/cm²)	Cross Section (cm²)	Cross Section Error
P3	A	5	2.39×10^{11}	3.93×10^{-11}	1.76×10^{-11}
P3	B	0	2.56×10^{11}	$< 9.59 \times 10^{-12}$	9.59×10^{-12}
P3	D	2	3.96×10^{11}	2.36×10^{-11}	1.67×10^{-11}
P3	F	2	3.92×10^{11}	2.02×10^{-11}	1.43×10^{-11}
P3	G	1	2.62×10^{11}	1.05×10^{-11}	1.05×10^{-11}

The main item to be seen in the above table is that very few events were actually observed for all the other test that were run. The cross sections calculated in this table are total cross section since, for all but test A, determining the number of effective bits is difficult. For test A, with five 32-bit registers being tested, a per-bit cross section is approximately 2×10^{-13} cm²/bit, slightly higher than the cache or tag cross sections, but there is quite a bit of uncertainty in that number due to the small number of events. While it is not satisfying to have so few upsets and large variations in cross section, it does imply that the sensitivity of upsets in these areas of the processor is small and of little concern for space operations.

Proton Summary Data

Cross Sections (cm^2 or cm^2/bit)

Legend:
- Data Cache Tags
- Caches
- Exceptions
- SEFIs

y-axis: 10^{-8}, 10^{-9}, 10^{-10}, 10^{-11}, 10^{-12}, 10^{-13}, 10^{-14}, 10^{-15}, 10^{-16}

x-axis: L1 Data Only   L1 Data & L2   All Cache On   All Cache Off

The above figure shows a summary plot of the data taken for this testing as a function of the cache state. It is very obvious here that the exception rate is dominant for the case using the instruction cache but not for the other cases. This lends a strong impression that exceptions, or exception type events, are not leading to SEFI events. This impression is strengthened by the fact that the SEFI does not increase dramatically for the all caches case, even when the exception rate does.

While it is not shown this way, if the instruction cache data were presented as a total cross section rather than a per-bit cross section, it's value would be approximately twice that of the exception cross section. Referring back to test E, approximately two-thirds of the instruction cache is tested and one-third is used for instruction space, or twice as much cache is tested as cache space that could lead to an exception. This implies that approximately every proton that produces an event in the instruction cache will lead to an exception. This makes sense, as the test conditions for test E would have to be considered heavy utilization of the instruction cache. For software that did not rely as heavily on the instruction cache, this ration would most likely be much less. The main point to take is the importance of exception handling when the instruction cache is utilized, since if these exceptions were not handled, the processor would halt, leading effectively to a SEFI event.

Heavy Ion SEFI Data
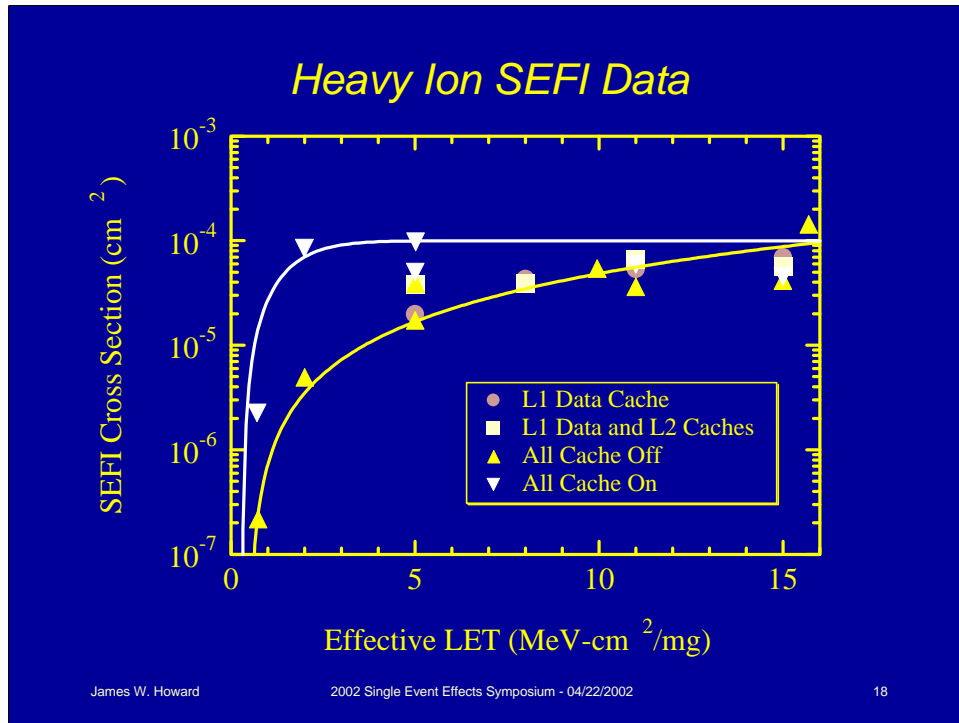
The above figure shows the SEFI cross section for all the parts tested as a function of the effective LET. Shown are four data sets representing the four cache conditions that were tested: All cache on, All cache off, L1 Data on only, and L1 and L2 Data cache on only. The first observation to make is that to first order the saturation cross sections for all cache conditions are in the same order of magnitude. While the "All Cache Off" case is consistently below the other cases, it is not significantly below, except possibly in the knee regions of the cross section curves. This data seems to indicate that the primary mechanism that leads to a SEFI event is not generated with an error event in the cache. The cache may play a role in a second order effect near threshold.

Heavy Ion SEE Data
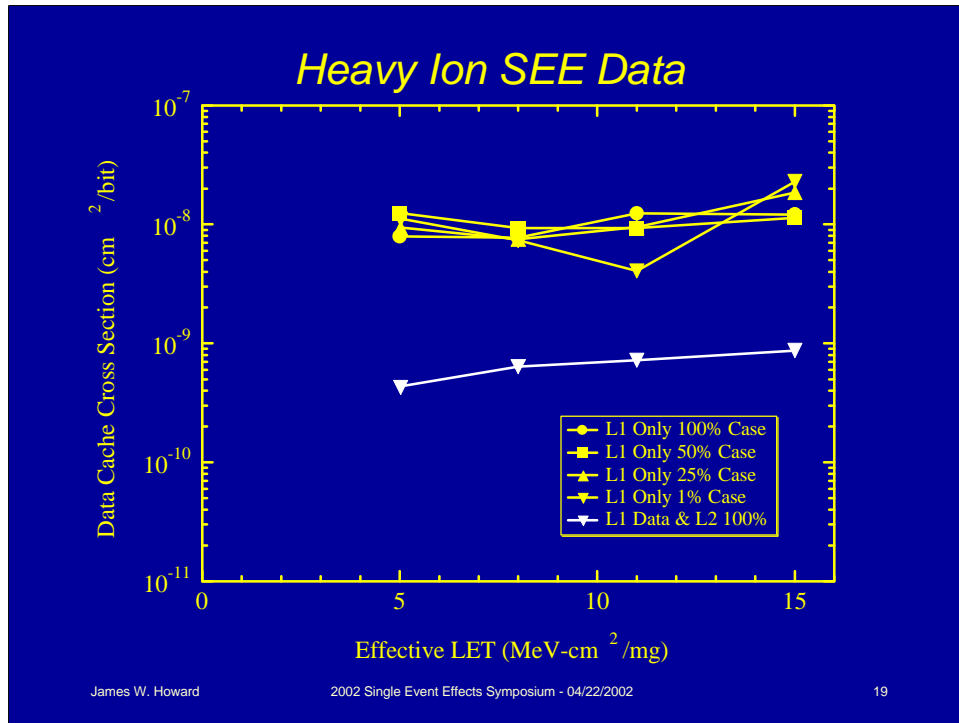
The same effect that was pointed out for the proton data (L2 cache percentage issue) was also observed with heavy ions. Proton testing demonstrated that the 100% curve for the L2 cache case contains the correct data. Plotted above is that data as well as the four percentage cases for the L1 data cache cases. As with the proton data, all four L1 data cache case curves fall on top of each other. Also, similar to the proton data, the L1 data cache curves are approximately an order of magnitude larger in cross section that the 100% case for the L2 cache.

Summary

- Extensive data has been collected on the total ionizing dose and single event response of the Intel Pentium III microprocessors.
- The data indicates:
  - high tolerance to TID
  - no susceptibility to SEL from protons or heavy ions to an LET of 15 MeV-cm^2/mg
  - Single event upsets and functional interrupts are present
- Care must be taken in testing parts like the P3 where it must be treated like a "black box". Our cache testing showed a dramatic difference in test results simply by how the cache is utilized.

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Extensive data has been collected on the total dose and single event response of the Intel Pentium III. The data indicates that there is a high tolerance to total dose and there is no susceptibility to latchup from protons and heavy ions to an LET of approximately 15 MeV-cm^2/mg. Single event upsets and functional interrupts are present. However, for the Pentium III, if running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment. The thermal issues and the power requirements of these processors will most likely be the limiting factors in their usage in space applications.