EVALUATION OF THE DIGITAL SIGNAL PROCESSOR TSC21020F
FROM THE MANUFACTURER TEMIC SEMICONDUCTORS MHS FOR SPACE APPLICATIONS

Marielle BELASIC [1-1], Françoise BEZERRA [1-2] , Guy ROUXEL [3]
(1) CNES 18, avenue Edouard Belin. 31401 TOULOUSE Cedex 4
(-1) Tel : 33 5 61 28 16 69 Fax : 33 5 61 28 13 30 e-mail : marielle.belasic @ cnes.fr
(-2) Tel : 33 5 61 28 21 53 Fax : 33 5 61 27 47 32 e-mail : francoise.bezerra @ cnes.fr
(3) MHS La Chantrerie. Route de Gachet. BP70602. 44306 NANTES Cedex3
Tel : 33 2 40 18 17 33 Fax : 33 2 40 18 19 60 e-mail : guy.rouxel @ temic.fr

Abstract

An evaluation of the Digital Signal Processor TSC21020F from the manufacturer TEMIC Semiconductors MHS for space applications has been performed. This evaluation has consisted of radiation tests, destructive tests, electrical characterization and endurance tests, in order to assess the specific failure modes and the reliability of this product in the space environment.
The different tests have shown :

- preservation of functionality, and parameters within specification limits, until 100krad (data got during development phase January 1998),
- no latch-up observed until 72MeV.cm^2/mg, and an improvement of a factor greater than 1200 in the SEU occurrence period in comparison with the standard ADSP21020 rev3.0 from Analog Devices,
- no major defect during the construction analysis,
- good functionality of the devices, and all static and dynamic parameters within specification limits, from power supply voltage 4.5V to 5.5V (20MHz) on the whole temperature range,
- no reliability problem during endurance testing.

So, these positive results have confirmed the ability of the TSC21020F to be used in space applications.

1. INTRODUCTION

In order to satisfy commercial space programs needs, like communication satellites constellations, CNES has carried out an evaluation of the Digital Signal Processor TSC21020F from the manufacturer TEMIC MHS to check if this product meets space requirements. The processor evaluation plan, including radiation tests, destructive and endurance tests has been developed in order to assess the manufacturing quality, the reliability of the component. These tests also intend to check the margins related to performances and reliability with regards to space missions.

The TSC21020F is a single-chip IEEE floating-point processor (32 bits) optimized for digital signal processing applications. Its design is pin and code compatible with the ADI ADSP21020 processors (agreement between Analog Devices and MHS). Fabricated in a high-speed, low-power and radiation tolerant CMOS process, the TSC21020F has a 50 ns instruction cycle time. With a high-performance on-chip instruction cache, the TSC21020F can execute every instruction in a single cycle time.

Hereafter, are presented the product maximum ratings and performance values :

Supply voltage	V_{DD}	-0.5 to + 7 V
Input voltage	V_{IN}	-0.5 to V_{DD} +0.5V
Output current	I_{OUT}	50 mA
Device dissipation	P_D	13 W
Operating temperature range	Top	-55 to +125 °C
Clock frequency	tckmin / tckmax	6 / 20 MHz
Supply current	I_{IDLE}	< 100 mA
Supply current	I_{DDIN}	< 480 mA

This product has been developped by a consortium between DASA/Dornier Satellitensysteme (prime contractor, responsibility for validating the DSP development), TEMIC Semiconductors MHS (major subcontractor, responsibility for the DSP chip development based on the ADSP-21020), and IMS2 (role of test house : radiation and electrical characterization) within the framework of an ESA/ESTEC contract.

The Radiation Tolerant technology (SCMOS2RTP) has been developed under CNES contract by modifying and adding some process steps. A First P+ implantation has been introduced for guards rings, to suppress the leakage currents between two N-type diffusions or between two NMOS transistors. A P-type implant is added in the N+ protection of the NMOS transistors to suppress the leakage current under the bird's beak regions. In addition, the implantation doses of the Pwell and Nwell have been adjusted to make this technology latchup immune, while keeping the diodes breakdown voltages high enough to fulfil normal applications.

In order to satisfy a high degree of availability and dependability in domains where the maintenability is difficult or even impossible, commercial space projects require devices exhibiting high quality and reliability levels.

The purpose of this ETP (evaluation Test Plan) is to check these characteristics and the available margins in order to satisfy such stringent missions.

The evaluation of this processor has consisted of quality reliability and radiation tests.

Reliability tests were intended to give informations us on the capability of these components to be used in space applications and to detect potential defects in order to apply adapted corrective actions.

Radiation tests were intended to check the following objectives :

-Total Ionizing Dose : preservation of functionality, and parameters within specification limits, until 100krads.

-Single Event Upset : no SEU for Linear Energy Transfert lower than 30 MeV.cm^2/mg.

-Latch-Up : no Latch-Up for Linear Energy Transfert lower than 70 MeV.cm^2/mg.

The markets targeted by this processor are worlwide space projects requiring high level of digital signal processing. ROSETTA, IASI, the space station experiments, GALILEOSAT are some potential examples, but also commercial programs like communication satellite constellations.

The work to be done was split as follows :

- parts manufacturing. The manufacturing plant (diffusion line, assembly and test) is located in Nantes. This step was completed in july 1999.

-evaluation of the DSP TSC21020F, including destructive tests, electrical and endurance tests.

2. PARTS MANUFACTURING AND SPECIFICATION DRAWING [1]

This step consisted in the product specification drawing according to ESA/SCC system (adaptation of the existing MHS internal specifications, and introduction of the table 7 for post irradiation parameters), and, in manufacturing and electrically characterizing the parts required for the evaluation.

The parts are processed on the MHS 0.6µm radiation tolerant technology SCMOS2RTP process 3 metal layers, and are assembled in 256-pin MQFP-F packages. The 256-pin MQFP-F package leads are manufactured with Iron-Nickel Alloy (alloy 42). The final finish of leads is gold plating, electro-deposited.

The components subjected to the tests were from a homogeneous manufacturing lot and produced according to the following requirements : the dice have been visually inspected in accordance with MIL-STD-883 method 2010 condition B, and a SEM inspection in accordance with ESA/SCC22400 has been performed on one part, which did not show any major defect. After pre-encapsulation of the lot performed by MHS, all the components have been submitted to a radiography inspection and to a pre-encapsulation internal visual inspection performed by CNES, which has been successfully done : the 83 parts of the lot have been accepted.

This screening has been followed by the final production tests, corresponding to ESA/SCC9000 CHARTII (Bond strength test, die-shear test, encapsulation, high temperature stabilization bake, temperature cycling, constant acceleration, marking + serialization, Pind test, seal test, dimension check, external visual inspection, and electrical measurements at room, high and low temperatures according to tables 2 and 3 of detail specification). At the issue of these tests, 76 parts were available.

Afterwards a CSI has been achieved including :

-electrical measurements at room, high and low temperatures on twenty parts,

-seal test and external visual inspection on twenty parts.

These DSP have been used later on for endurance testing.

In addition, solderability and marking permanency tests have been performed on five other pieces.

All these tests have shown positive results.

3. COMPONENTS EVALUATION [2]

The evaluation testing was derived from ESA/SCC2269000 standard. Fifty-six Digital Signal Processors were required to do this evaluation. The components were divided in four groups :

-control group : the control group was composed of 3 parts, which were used as control parts for each sub-group. The data were compared to initial and were used for test set-up validations.

-destructive tests : SEU/SEL testing, construction analysis, ESD sensitivity, and electrical characterization (functionality, a.c/d.c parameters, electrical latch-up, breakdown voltage, thermal resistance)

-endurance tests

-reserve group : five parts were kept for further investigations.

The destructive, electrical and endurance results are detailed in the following paragraphs.

3.1 Destructive and electrical tests

A. Destructive tests

Several tests are included in this category :

A.1 Radiation tests : Total Ionizing Dose and SEU/SEL testing.

a)Total Ionizing Dose

No total dose test has been performed.

Data got during the development phase carried out by IMS2 at DCN/Indret close to MHS plant in Nantes, on 13-22 January 1998, were credited : 8 parts have been irradiated at 15, 30, 50, 75 and 100krad (2 parts were taken as reference parts) ; after irradiation, a double annealing was performed : 24H at 25°C followed by 168H at 100°C. Results are presented hereafter : no significant or relevant drift for all parameters, only very minor degradations in current consumption at 100krad : IDDIN (internal supply current) maximum drift is 15mA (3.5%), IDDIDLE (supply current in mode stand-by) maximum drift is 20 mA (average 15mA).

So, the product fully reaches the total dose objectives (>100krad).

b) SEU/SEL testing

For the SEU/SEL tests, five parts (samples from prototype lots) encapsulated in PGA packages (according to MHS quality flow used for engineering samples) have been used. The tests have been done from January till October 1999 on the Van de Graaff Tandem of the Institut de Physique Nucléaire (IPN – Orsay France) and on the cyclotron of the Université Catholique de Louvain (UCL - Belgium) according to ESA/SCC25100. These tests have permitted to compare the product TSC21020F with the ADSP21020 die rev 3.0 from Analog Devices (DC9609 KG80 3.0).

The SEE test system and test conditions used are only briefly described, as a paper presented at RADECS'95 by F.Bezerra covers these issues **[5]**. The test consists in running a program on the processor while it is exposed to radiation and checking its 'real time' operating characteristics, and controlling the power supplies using a latch-up detection system. The test programs can be static or dynamic. For static ones, for 90% of the program's duration the state of the processor is fixed and SEUs accumulate. The values are then read and compared with the initial values. In contrast, during the dynamic tests, the processor is not fixed in a preferred state. These tests are generally short application programs which use the processor different features one after the other. Latch-up detection is carried out by monitoring the current (threshold exceeded for a given time) and the voltage (stability of power supply voltage).

Static tests on registers, internal cache memory and address generators have been done on SEU and Latch-up tester for microprocessors developped by CNES, and able to test complex components. The operating frequency during testing was 20MHz.

The results are presented in a summary format, and are given for the following orbits :

-Heliosynchronous (SPOT) : 800km, 97°.

-geostationary (GEO) : 36000km, 0°.

- (TOPEX) : 1300km, 60°.

b.1) Latch-up

The latch-up detection threshold was set at 30mA above consumption. No Latch-up has been observed on the TSC21020F up to 72 MeV.cm^2/mg.

In comparison, for the ADSP21020 processor from Analog Devices, the LET threshold is 32 MeV.cm^2/mg : the period of occurrence of a Latch-up is 11,5 years in geostationary orbit, 43 years in SPOT orbit and 62 years in TOPEX orbit.

b.2)Upset

The periods of occurrence of a SEU on registers are presented in the following table for the 3 orbits :

Orbit	**ADSP21020**	**TSC21020F**
GEO	43 days	143 years
SPOT	141 days	500 years
TOPEX	177 days	670 years

At the component level, the program register test gives the most pessimistic results.

For the other tests (cache memory and address generator), the TSC21020F is very low sensitive, and the rate of events in orbit could not be calculated. Measurements done allow us to say that compared with the ADSP21020rev3.0, the saturated cross-section for the cache memory is divided by 30 and by 10 for the address generator of the TSC21020F.

In addition, FFT tests were known to be less sensitive than static ones and have not been performed on TSC version.

From these results, it is concluded that the TSC21020F from TEMIC MHS leads to an upset occurrence period improvement by a factor greater than 1200 in comparison with the ADSP21020 rev3.0 from Analog Devices.

A.2 Construction analysis

This activity has been undertaken by CNES **[4]**. The Back-end (die-attach, bonding, encapsulation,…) and the Front-End (technology identification) have been analysed on ten parts.

The result is positive : no major defect has been revealed.

This analysis consisted of :

- an internal vapor analysis on 3 parts. The components have been sealed in N2/H2 atmosphere. The moisture content was satisfactory (lower than 700ppm),
- the Xrays inspection showed porosities in the die-attach (due to silver glue material), within MIL-STD-883E method 2012 requirements,
- the internal visual inspection was satisfactory, in spite of the presence of little resin on the pads sides,
- the MEB inspection (according to MIL-STD-883E method 2010) and the passivation integrity test (according to MIL-STD-883E method 2021) have been successfully done : good ultrasonic wire bondings on the die, and on the package side ; no defect has been detected,
- during the bond pull test (according to MIL-STD-883E method 2011), the wires broke for a strength greater than the one required by the specification : 3.5gm (average) (2gm specified for a 30µm wire),
- a SEM inspection including microsections, to analyse the front-end, will be done in the next weeks. It is reminded that results obtained on previous products from MHS have shown no major defect.

A.3 Package tests

No package related tests were foreseen in this evaluation plan (tests already performed under other evaluation testing). This activity has been undertaken in the framework of the MCRT capability approval. Results were satisfactory

A.4 Electro Static Discharge sensitivity

Human Body Model has been applied according to MIL-STD-883E method 3015.7. Failure has occured at 3000V thus validating the product MIL-STD class 2 classification.

B. Electrical tests

Ten parts of the lot have been successfully submitted to an electrical characterization : the functionality and the a.c/d.c parameters have been verified over the military temperature range (-55°C up to +125°C) with power supply voltage from 4.5V up to 5.5V(20MHz).

No concern about the breakdown voltage characterized at ambiant temperature ; the parts remained functional after this test.

Three other parts have been subjected to a thermal resistance measurement (junction to case) according to MHS procedure agreed by ESTEC. The result is 3.3°C/W (average).

No electrical Latch-Up has been measured on the five tested parts.

3.2 Endurance tests

It is reminded that those tests are performed so as to try to trigger failure modes using condition far beyond the maximum ratings for which the product is specified.

Twenty DSP have been used for endurance testing in order to assess the reliability and the specific failure modes of this product.

A. Life test at 140°C during 2000H

Ten parts have been submitted to a life test at 140°C during 2000H according to burn-in schematic and conditions given in table 5 of detail specification (execution continuously of a single instruction, coded on 48 bits, which stimulated the multiplier, the arithmetic and logic unit, and a program memory data access). Electrical points have been measured at :

-168H (-55, 25, 125°C) according tables 2 and 3 of detail specification,
-500H (25°C) according table 2,
-1000H (25°C) according table 2,
-2000H (-55, 25, 125°C) according tables 2 and 3 of the detail specification.

No reject occurred during this test.

A parametric drift analysis at room temperature has been performed between the data obtained at initial measurement and at : 168H, 500H, 1000H, 2000H according table 4 of the detail specification, and no significant drift has been noticed.

B. Life test at 175°C during 3000H

Ten other parts have been submitted to a life test at 175°C during 3000H according to burn-in schematic and conditions given in table 5 of detail specification. Electrical measurements have been done at :

-168H (-55, 25, 125°C) according tables 2 and 3 of detail specification,
-500H (25°C) according table2,
-1000H (25°C) according table2,
-2000H (25°C) according table2,
-3000H (-55, 25, 125°C) according tables 2 and 3 of detail specification.

The DSP have shown no reliability problem. The parts have successfully passed the endurance test.

A parametric drift analysis at room temperature has been performed between the data obtained at initial measurement and at : 168H, 500H, 1000H, 2000H, 3000H, according table 4 of the detail specification. All the parts passed the test and no major concern has been noticed.

As the evaluation results are satisfactory, a Process Identification Document (PID) have to be established, in which all the manufacturing and control specifications, and instructions will be included.

Therefore, this product has been proposed and introduced in the part I of the European Preferred Parts List (EPPL).

4. CONCLUSION

This evaluation testing derived from ESA/SCC 2269000 standard has shown :

-all static and dynamic parameters passed the test limits specified in detail specification, within the whole temperature range, and with power supply voltage from 4.5V to 5.5V(20MHz).

-the Digital Signal Processors showed no reliability problem after the two endurance tests.

-no latch-up has been observed until 72MeV.cm^2/mg. For the Upsets, the program register test which gives the most pessimistic results, has induced periods of occurrence of an event greater than one hundred years for the geostationary orbit.

-no major defect has been detected during the construction analysis.

This demonstrates the robustness of the technology and the design.

So according to these positive results, the TEMIC MHS TSC21020F Digital Signal Processor is well suited for space applications.

References

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[2] HDBK9937 dated 30/12/1999. Three volumes. Lot 2 : ‘Evaluation for space use of the DSP TSC21020E MHS/SCC040’. Lot number Z26749. Contract n°721/98/cnes/7506/00.

[3] Radiations report to be writen (DTS/AQ/EQE/ER).

[4] Construction analysis report DTS/AQ/EQE/AE-2000/0060.

[5] F. Bezzera, D. Hardy, R. Velazco, and H. ZIADE 'TILMICRO, a new SEU and Latch-up tester for microprocessors. Initial results on 32-bit floating point DSPs'. Paper presented at RADECS September 1995 Arcachon France, p296-301.